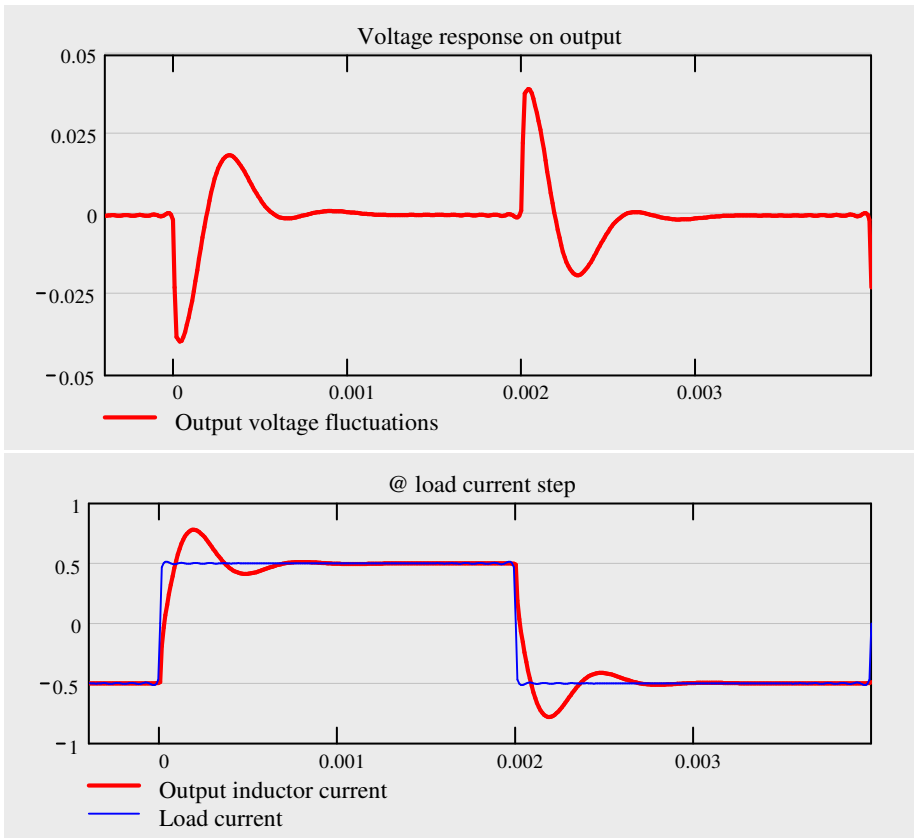


Load your network variables here:

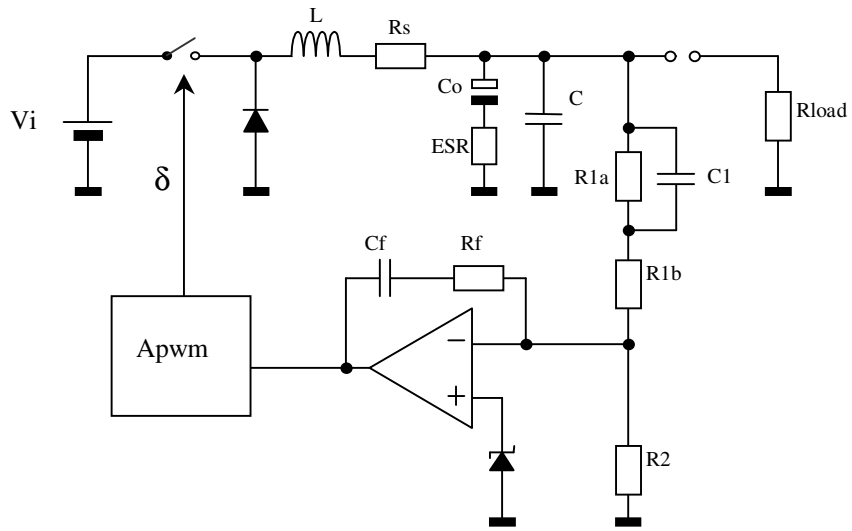
- Pulse width modulator gain: $A_{pwm} \equiv 0.5$ [V⁻¹]
- OP AMP gain * bandwidth: $f_{0dB} \equiv 1 \cdot 10^6$
- OP AMP feedback resistor: $R_f \equiv 22 \cdot 10^3$
- OP AMP feedback capacitor: $C_f \equiv 10 \cdot 10^{-9}$
- Upper resistor in voltage divider: $R_{1a} \equiv 33 \cdot 10^3$
- Capacitor in parallel to R1a: $C_1 \equiv 2.2 \cdot 10^{-9}$
- Middle resistor in voltage divider: $R_{1b} \equiv 5 \cdot 10^3$
- Lower resistor in voltage divider: $R_2 \equiv 10 \cdot 10^3$
- Output capacitor: $C_o \equiv 1000 \cdot 10^{-6}$
- ESR in output capacitor: $ESR \equiv 0.045$
- C || output capacitor: $C \equiv 0$
- Dynamic load resistance: $R_{load} \equiv 100$
- Output inductor: $L \equiv 100 \cdot 10^{-6}$
- ESR in output inductor: $R_s \equiv 0.02$
- Input voltage: $V_i \equiv 50$

Loop circuit diagram: see next page.

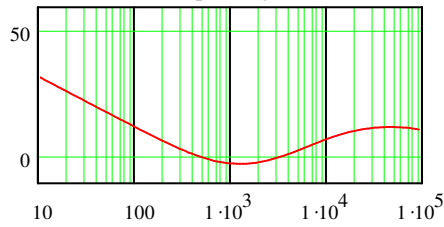
- Test frequency: $F_o \equiv 250$ [Hz]
- Current step size: $I_{step} \equiv 1$ [A]



Buck converter. Voltage mode control.



Error amplifier gain [dB]



Error amplifier phase

