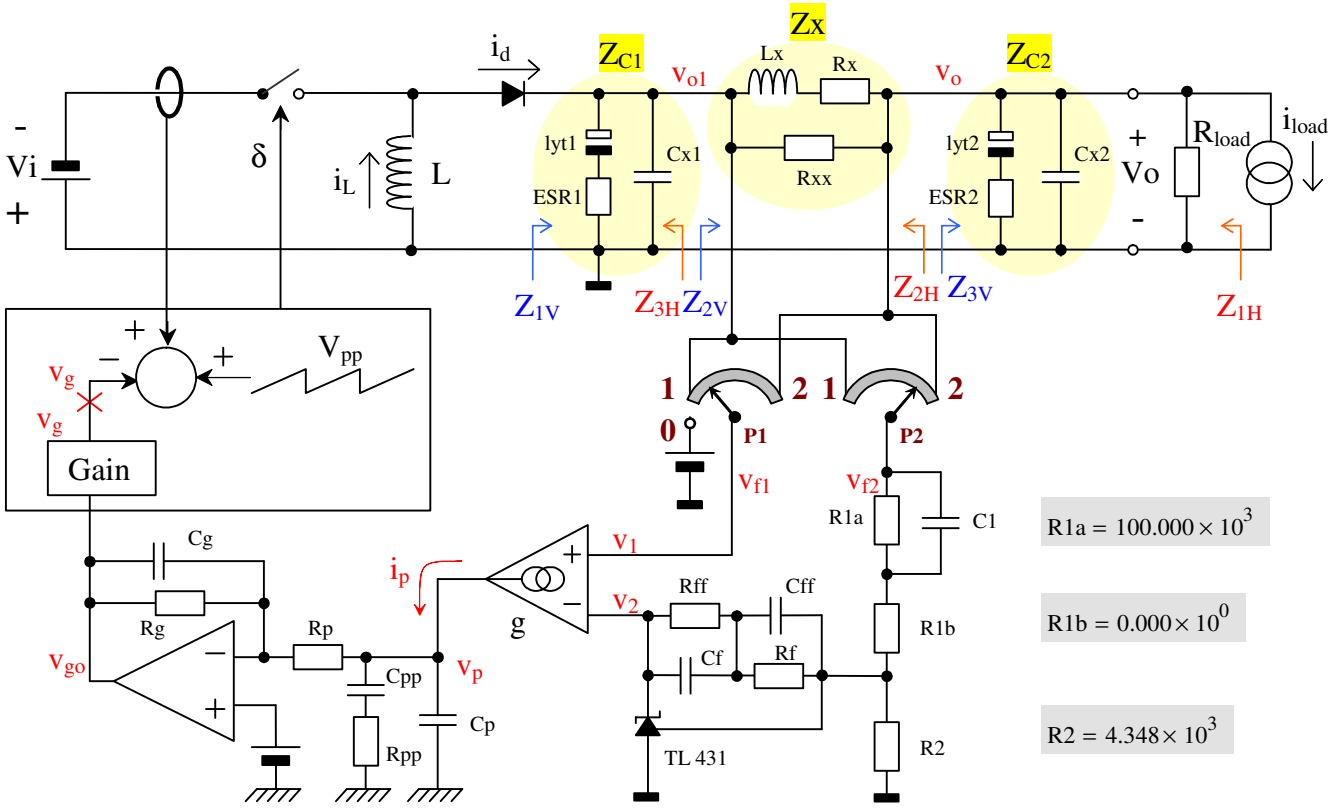
Loop gain in a Buck-Boost converter with current mode control and slope compensation.

calculation routine

Buck-boost converter with output LC filter.
Continuous or discontinuous current.
Current mode control with slope compensation.



$R1a = 100.000 \times 10^{3}$

$R1b = 0.000 \times 10^{0}$

$R2 = 4.348 \times 10^{3}$

Logarithmic frequency sweep:

Switching frequency: $F \equiv 100 \cdot 10^{3}$

Min. and max. frequency: $fmin \equiv 10$ $fmax \equiv 1 \cdot F$

Number of points pr. decade: $N \equiv 50$ $i \equiv 0, 1 .. N \cdot \log\left(\frac{fmax}{fmin}\right)$ $f_i \equiv fmin \cdot 10^{\frac{i}{N}}$

Load your network variables here:

Inductor: $L \equiv 300 \cdot 10^{-6}$

First output capacitor: $lyt1 \equiv 220 \cdot 10^{-6}$ $Cx1 \equiv 0 \cdot 10^{-6}$
$ESR1 \equiv 0.05$

Filter inductor: $Lx \equiv 5 \cdot 10^{-6}$ $Rx \equiv 0$
$Rxx \equiv 44$

Filter capacitor: $lyt2 \equiv 220 \cdot 10^{-6}$ $Cx2 \equiv 0 \cdot 10^{-6}$
$ESR2 \equiv 0.05$

Load resistance: $Rload \equiv 10000$

Error amp. gain ∗ bandwidth: $f0dB \equiv 2 \cdot 10^{6}$

Error amp. feedback resistor: $Rf \equiv 220 \cdot 10^{3}$

Error amp. feedback capacitor: $Cf \equiv 2.2 \cdot 10^{-9}$

Low load stability resistor: $Rff \equiv 10^{10}$

Ripple suppression capacitor: $Cff \equiv 100 \cdot 10^{-12}$

Upper resistor in voltage divider: $R1a \equiv 100 \cdot 10^{3}$

Capacitor in parallel to R1a: $C1 \equiv 0$

Middle resistor in voltage divider: $R1b \equiv 0$

Voltage divider output: $Vref \equiv 2.5$

Transconductance gain [A/V]: $gm \equiv 0.001$

gm amplifier load resistance: $Rp \equiv 0$

Noise capacitor || Rp: $Cp \equiv 0$

R+C || Rp and Cp: $Rpp \equiv 0$
$Cpp \equiv 0$

Prim. amp. feedback resistor: $Rg \equiv gm^{-1}$

Prim. amp. feedback capacitor: $Cg \equiv 0$

Slope compensation ramp: $Vpp \equiv 0.05$

Current mode constant [V/Apeak]: $Rsens \equiv 0.1$

Fixed modulator gain: $Gain_g \equiv 0.61$

Feedback connection points: $\begin{pmatrix} P1 \\ P2 \end{pmatrix} \equiv \begin{pmatrix} 0 \\ 1 \end{pmatrix}$
P1 = 1- 2 or 0 **P2 = 1- 2**

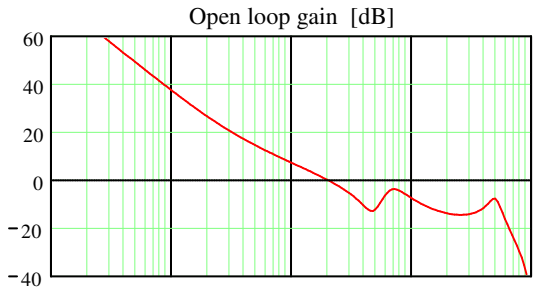
Input voltage: $Vi \equiv 50$

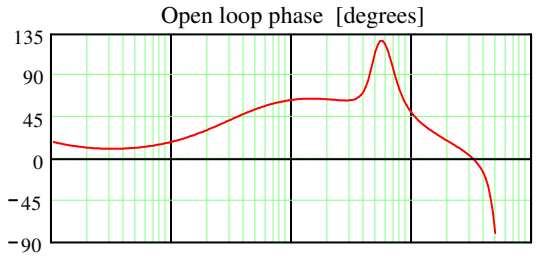
Output voltage: $Vo \equiv 60$

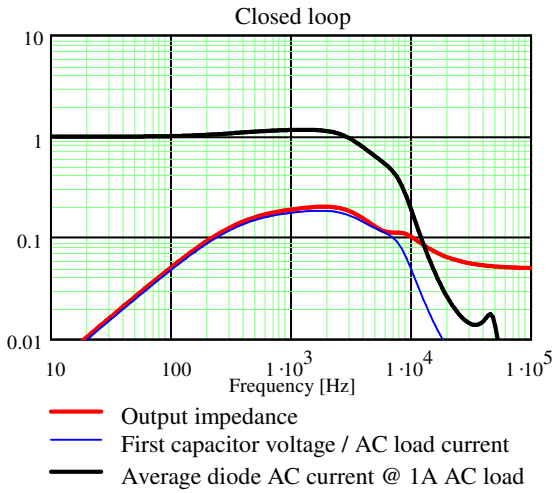
Power: $P \equiv 40$ [W]

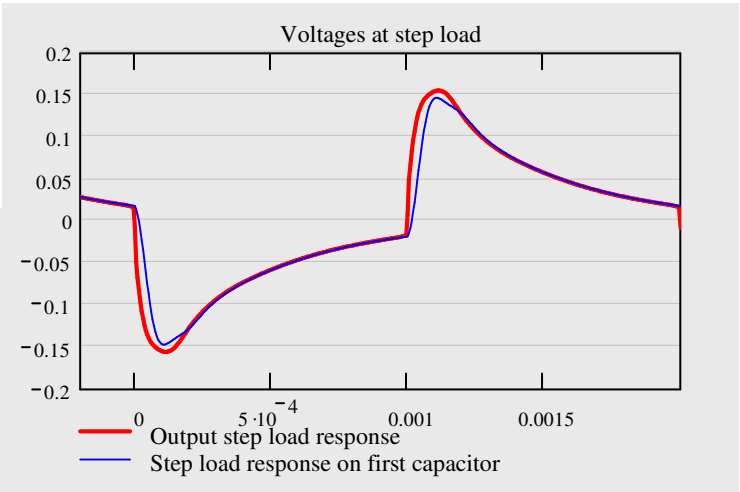
Test frequency: $Fo \equiv 500$ [Hz]

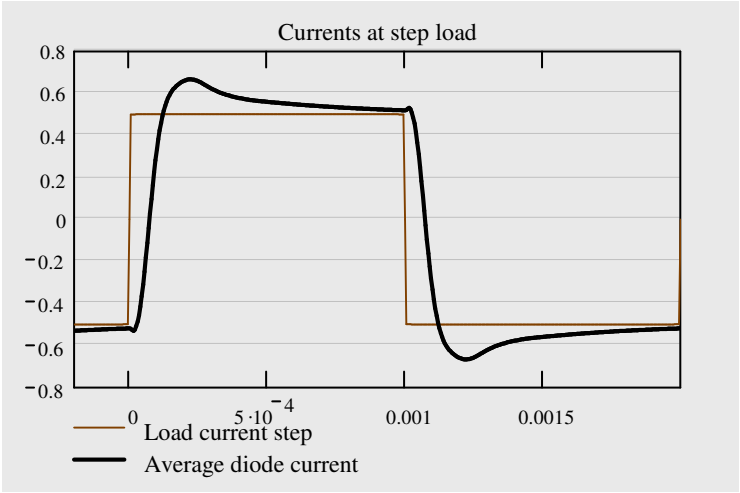
Current step: $Istep \equiv 1$ [A]











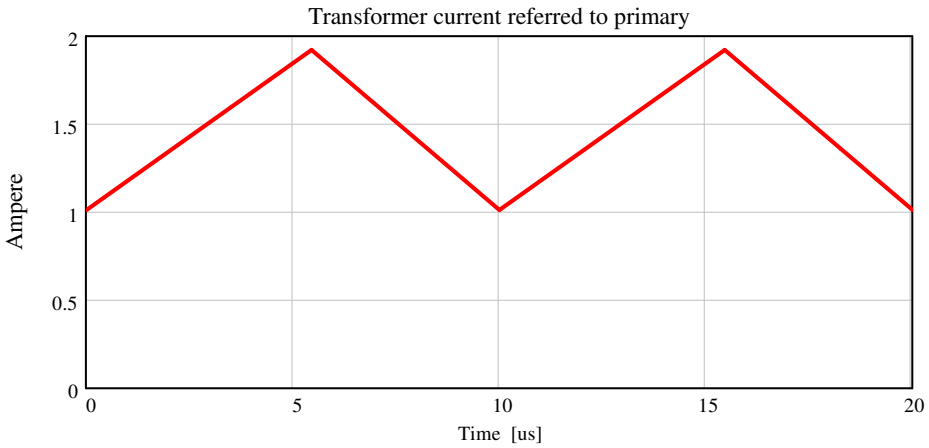
Right half plane zero [kHz]: $rhpZero = 18.1 \times 10^3$

Relative slope: $\frac{slope}{downslope} = 0.25$

Minimum slope for stability in CCM: $\frac{min\_slope}{downslope} = 0.08$

Sub resonance warning: $pro = -0.69$

$pro \le -1$ means unconditional subharmonic oscillation.
$-1 < pro < -0.5$ is inherently stable but can become unstable when the outer feedback loop is closed.



Mode = "continuous current"

User guide.

This worksheet calculates open loop (small signal) gain + phase and closed loop properties of a buck-boost converter.
It also shows you the response to a step load at a selected frequency and amplitude.
The converter can be in continuous current or discontinuous current mode. The control scheme can be voltage mode (duty cycle control) or current mode control with any slope compensation.
Units are [Volt], [Ampere], [Ω], [Henry], [Farad], [seconds], [Hz].

Once you have made your choices of input data, the worksheet will show you what mode you are in, and for current mode control it will indicate if you have enough slope compensation for subharmonic stability.
Voltage mode control is when you set Rsens = 0. Pure current mode control is when you set Vpp = 0.
In continuous current mode (CCM) you need slope compensation above 50% duty cycle. Insert Vpp > 0 to add slope compensation. The more slope compensation you use, the more you will approach the properties of duty cycle control.
This new worksheet also includes a model of the "sampled" sub-harmonic ringing or instability at F/2 in current mode control.
You can de-select this model by setting sub = "no" which gives you the possibility to study the additional effect and extra accuracy of the sub-harmonic modelling in CCM.

The loop behaviour may depend strongly on the steady state operating condition of your buck-boost converter.
You should do the calculation at low and high power and at low and high input voltage and assure that your design is stable in all working conditions.
If you use electrolytic capacitors in the output you should also test your design with low ESR and high ESR (in cold capacitors the ESR may increase tenfold). Low ESR can give loop problems at medium frequencies, high ESR can give you problems at high frequencies.

There is usually a high ripple voltage on the output of a buck-boost converter, hence an LC ripple suppression filter is often used. This filter may have dramatic influence on the loop performance. The worksheet includes several possibilities of connecting the feedback network to this filter, defined by the vector $\begin{pmatrix} P1 \\ P2 \end{pmatrix}$. Stability is often best, if P1 = 1. DC regulation is perfect, when P2 = 2. Usually this is the best choise. If the error amplifier has only one input, set P1 = 0.
In cases where output capacitors are not very large the output filter can create resonance at critical frequencies. If you adjust P1 and/or P2 between 1 and 2 you can sometimes cancel this resonance in the feedback loop so that the loop does not know about it. But the resonance will still be present in the closed loop output impedance. Often you can minimize filter ringings by adjusting P1 and P2 slightly lower than this cancellation point. But be careful - this design technique is very sensitive to tolerances.
It is a good idea to start the loop analysis without an inductor in the LC filter, and then when the loop looks nice you insert the filter and play with the feedback connection points. You may also have to damp the filter with Rxx.

If you use duty cycle (voltage mode) control in discontinuous current mode the loop calculator is not accurate due to the dead time ringing in the inductor + parasitic capacitances. Loop gain can be very dependent on whether the switch turns on in a ringing valley or on a ringing top.
Current mode control is insensitive to the dead time ringing.

Always verify the calculations by experiments. You can perform an open loop gain/phase analysis if you have an analyzer for that, or you can check the size and shape of the step load response.