LLC resonance half bridge converter

The LLC resonance converter is not widely used in the industry, but some companies have become quite attracted to it due to its potentially high efficiency and low EMI.
However the LLC converter is extremely difficult to comprehend, analyse and optimise. Those few engineers and scientists who are familiar with it, seem to stick to the so-called Fundamental Harmonic Analysis method in the frequency domain, some times combined with others like Pspice. Methods that are only partly accurate, in particular at low power, and which may seem to be slow and cumbersome to use.
Until to-day, I believe, no fast and direct design tool has ever been created for the LLC converter.

This mathematical worksheet was constructed for fast and accurate steady state analysis of LLC half bridge or full bridge resonance converters. The worksheet calculates scope pictures of currents and voltages in any working condition, and moreover it gives an overview of a lot of important parameters, e.g. switching frequency and rms currents plotted against power and input voltage. You only have to enter values for the three components C, Ls and L.

A basic schematic of an LLC converter is shown in figure 1, and an even more simplified representation is shown in figure 2 which we will use for the analysis. For simplicity the transformer is assumed to be ideal with a turns ratio of 1:1. After the analysis it is simple to modify the results to take a transformation ratio different from 1:1 into account.

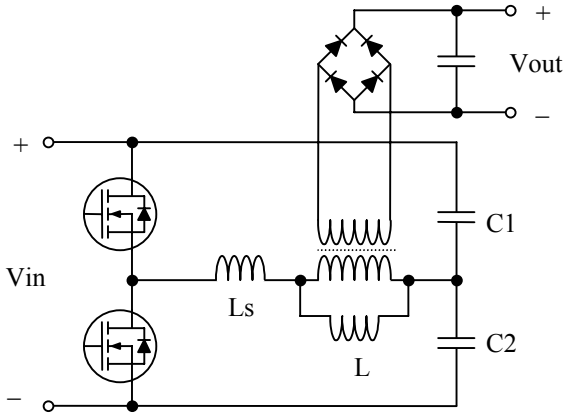


Figure 1

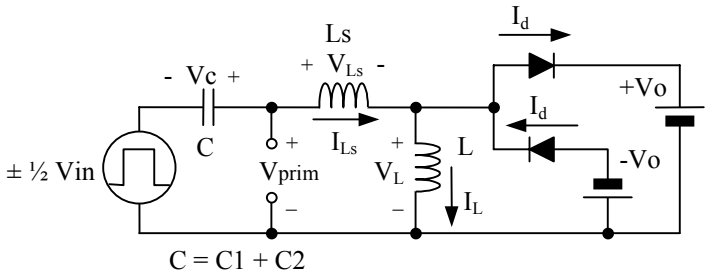


Figure 2

The worksheet uses an iteration process, which deals with analysis of the LC resonance waveforms in the time domain, assuming that input power = output power, i.e. a lossless circuit. These waveforms always consist of fractions of sines or cosines at one of the two resonance frequencies, that a lossless LC circuit must obey. One resonance frequency ω_o is present in those time intervals, where no output diode conducts. The other and higher resonance frequency ω_{oo} is present, when one of the output diodes conducts.

In an LLC converter the frequency is variable, however it appears that frequency will become constant over parts of the load range (this fact is not predicted by the Fundamental Harmonic Analysis, I believe). Therefore we cannot use the operating frequency as the input parameter for the analysis. Instead the capacitor start (and end) voltage Vc is chosen as the input parameter, since this voltage will somehow follow the transferred power. Then the operating frequency can be found as one of the results of the analysis.
The capacitor start voltage is therefore fixed during the iterations, only currents and times are manipulated by the iteration process.

The analysis is done only during one half period of operation, in which the input voltage is positive.
It starts at time = 0.
First we divide the half period 0 - T/2 in five sub-intervals with the following properties :
[0 - t1] : in this interval - if present - current initiated in the previous half period is still flowing in an output diode.
[t1 - t2] : this is an interval without diode current.
[t2 - t3] : usually the most important interval for diode rectification. This interval is always present.
[t3 - t4] : no diode currents flow.
[t4 - t5] : a short interval in the last part of a half period, in which the opposite diode (of that during t2 - t3) conducts.
t5 (= T/2) is the end of the half period, i.e. t5 is where the calculation ends.

The calculation starts with initial values at time = 0 of the three state variables : two inductor currents and one capacitor voltage.

Based on guessed initial state variables the times t1 - t4 and their associated currents and voltages are successivly calculated, and finally t5 is calculated as the time, at which the input state variable (capacitor voltage) is identical to its initial value but opposite in sign.

At time = t5 the two remaining state variables (inductor currents) must also be identical in size but opposite in sign to those at time = 0. They are usually not, because our first guess was of course not the right one. Based on the initial and the finally calculated values new and better current guesses for the next iteration are made, and the iteration process is continued, until initial and final values match with a small enough error.

The LLC converter is difficult to analyse accurately, because it can work in as much as 6 useful operating modes (even more modes exist, but they are less interesting, among others because they work with hard switching.) The only time interval present in all 6 modes is [t2 - t3]. The remaining intervals can be non existing. Which intervals are present depends on which mode we are in. In mode 6, as an example, the only intervals are [0 - t1] and [t2 - t3].

We never have more than 3 non-zero intervals at the same time. So why do we define 5 time intervals, which seems to be unnecessarily complicated ? The reason is that in each of the above mentioned time intervals - if existing - the currents and voltages always follow the same mathematical expressions. So at the end of the iteration all data can be extracted and handled by the same formulae, regardless of which mode we are in. In the end this was a great simplification.

The analysis can be split up in two distinct areas :
1) Vin < 2 ∗ Vo.
2) Vin > 2 ∗ Vo.
In area 1) there are 4 useful modes : 1, 2, 3 and 4. Mode 1 is present at low power transfer. The higher modes appear at higher power levels.
In area 2) there are 3 useful modes :1, 5 and 6. Again mode 1 is associated with the lowest power, and mode 6 with high power.

Strictly speaking there is also a mode 0, in which the operating frequency is higher than the frequency of no-load. The chosen method of analysis, where capacitor start voltage is the input parameter cannot show mode 0. Fortunately mode 0 is not very interesting, since mode 0 has no power transfer.

The magic point Vi = Vo (Vi = ½ ∗ Vin is input square wave amplitude) is by some designers referred to as "the load independent point". This point appears, if we operate the converter exactly at its (highest) resonance frequency ωoo, which is the resonance frequency of Ls and C. However the statement "load independent" is only completely true at high power, i.e. in modes > 1. At low power the output voltage does rise a bit. The load independent property can be understood by realizing that Ls + C become a short circuit at their resonance frequency, and therefore the input will be "connected" to the output, no matter how high currents are flowing. However at low power the diodes do not conduct all the time, so the rectified voltage will rise some % if frequency is kept constant.

Another important key operating point for the LLC converter is the point of loss of no-load operation. The range where the LLC converter can deliver zero load current is $Vi < Vo \cdot \frac{Ls + L}{L}$. However, as we approach $Vi = Vo \cdot \frac{Ls + L}{L}$ no-load requires the operating frequency to go towards infinity. The more Vi exceeds this limit, the higher will be the practical minimum controllable power (without the output voltage rising). A consequence of this is, that at short circuit there will always be some output current. We cannot have zero output voltage and current simultaneously.

Calculation of oscilloscope plots of currents and voltages.

Now we will show calculated examples of currents and voltages in all 6 modes. That will illustrate the LLC behaviour much better than words alone.
In the examples the following values have been used.

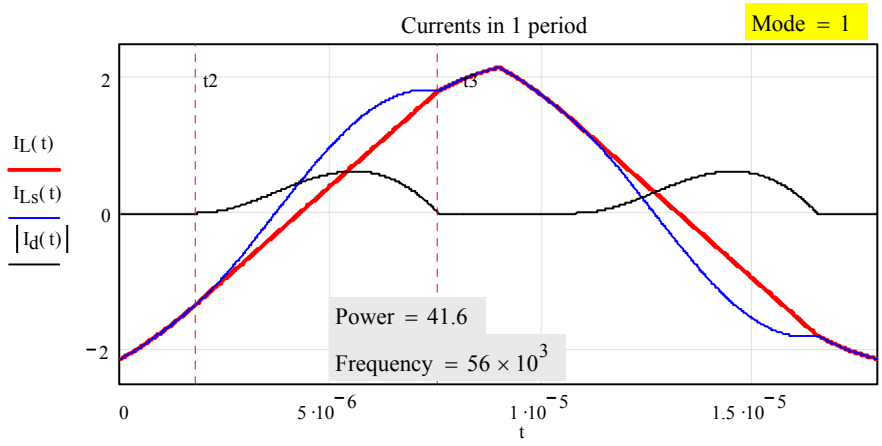
Selected component values : $C \equiv 30 \cdot 10^{-9}$ $Ls \equiv 172 \cdot 10^{-6}$ $L \equiv 344 \cdot 10^{-6}$
Fictitious output voltage (1:1 trafo) : $Vo \equiv 188$

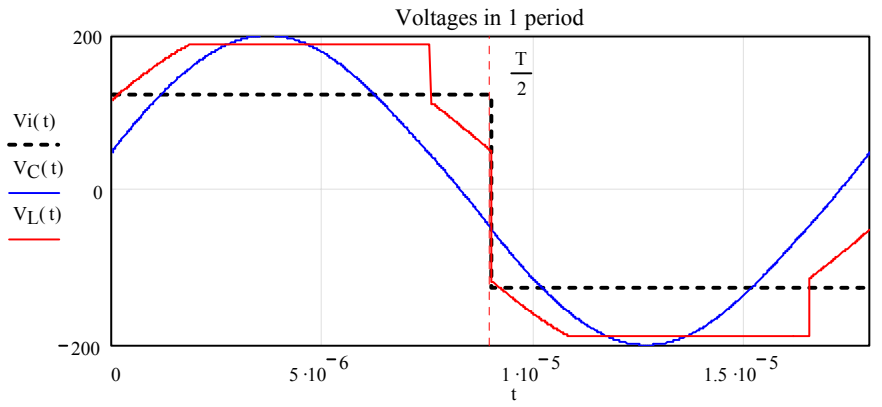
Capacitor voltage @ switching : $Vc \equiv 50$

Input voltage : $Vin \equiv 250$

In mode 1 the diode current has dead bands before and after switching.
The voltage on the diode has "shoulders" on both sides.
Note that rectification occurs in the time interval [t2-t3].

Mode 1 appears at low power for all input voltages.





Vi(t) is input square wave voltage ±½Vin.

You can see that capacitor voltage (blue trace) starts at 50V as specified and ends the half period at -50V.

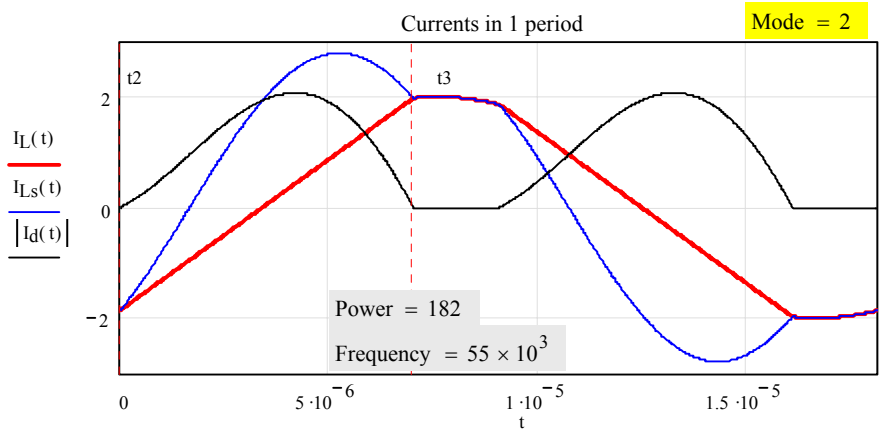
Capacitor voltage @ switching : $Vc \equiv 220$

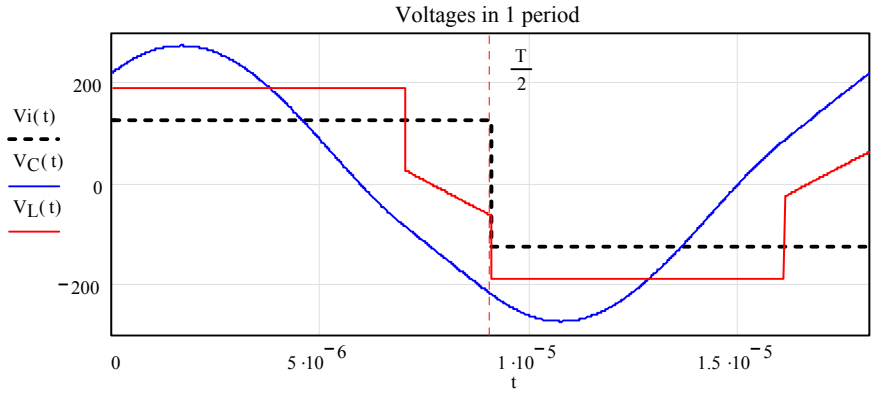
Input voltage : $Vin \equiv 250$

In mode 2 the diode current starts immediately after switching.
The voltage on the diode has a "shoulder" only on the right side.

Mode 2 appears at higher power for input voltages **Vin < 2 ∗ Vo.**

It is remarkable how little the frequency has gone down from mode 1 to 2, even though power has increased more than 4 times.

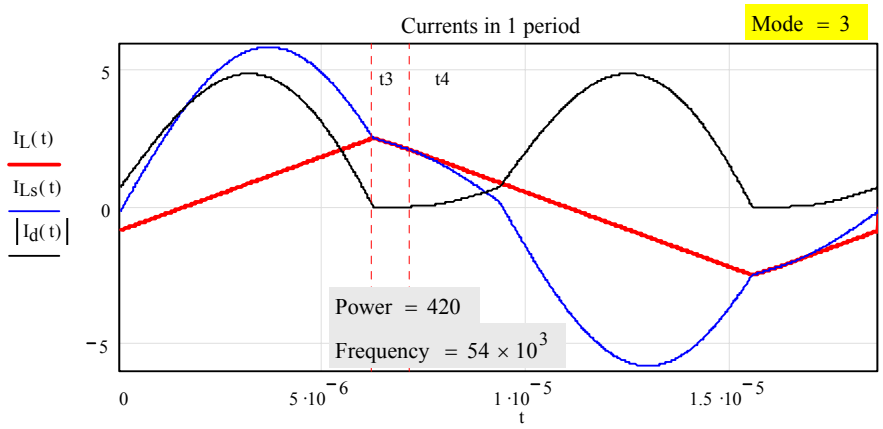


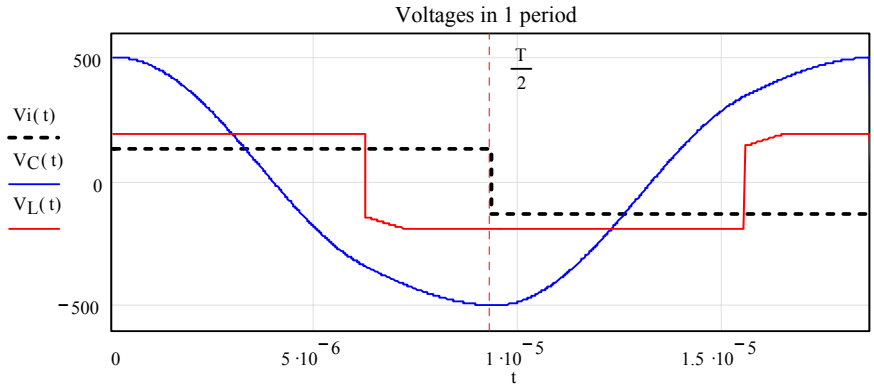


As the power increases the right voltage "shoulder" moves downwards, until its lowest part hits -Vo before the end of the half period. This is the start of mode 3, in which diode current starts at t4 already before switching.
In the voltage waveform we still see a small part of the shoulder remaining.

Capacitor voltage @ switching : Vc ≡ 500

Input voltage : Vin ≡ 260



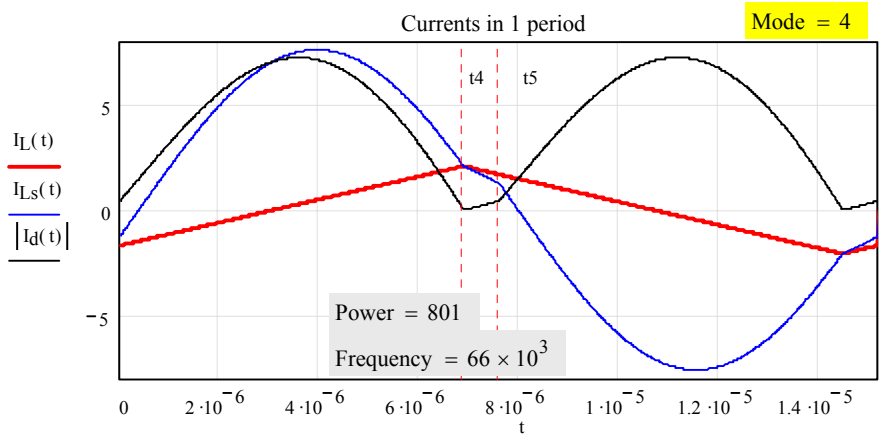


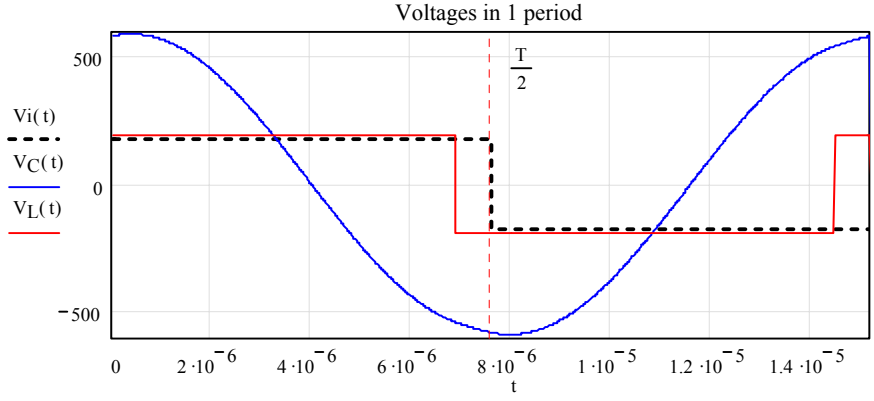
Going a little further up in power we some times arrive at mode 4, where the "shoulder" has completely disappeared. There is no more diode current dead band.

Mode 3 or mode 4 end at the maximum possible power transfer, which is limited when Vin < 2 ∗ Vo.

Capacitor voltage @ switching : Vc ≡ 580

Input voltage : Vin ≡ 350

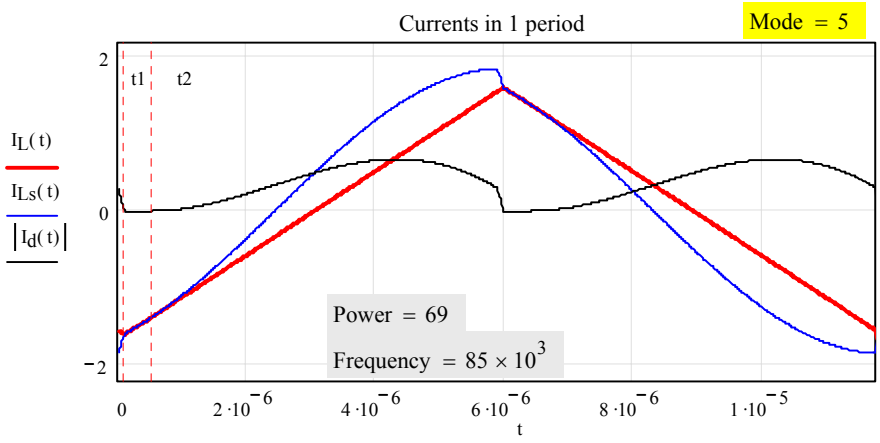


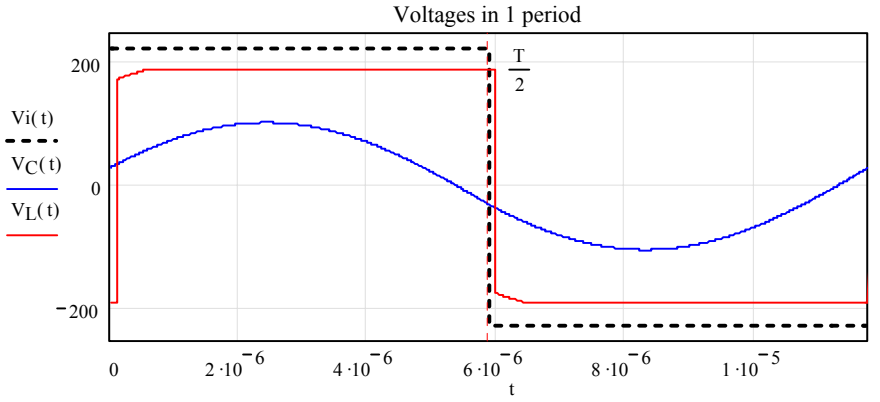


Capacitor voltage @ switching : Vc ≡ 30

Input voltage : Vin ≡ 450

Mode 5 appears after mode 1, if **Vin > 2 ∗ Vo**, which is the so-called load independent point. In this example this point lies at 2 ∗ Vo = 376V.
The voltage on the rectifier now has a tendency to be shifted to the right, so that at switching there is still current left in the bottom diode. This current ends at t1, then there is a small dead time, before the top diode starts conducting.
In the dead time we see a small "shoulder" on the left voltage edge.



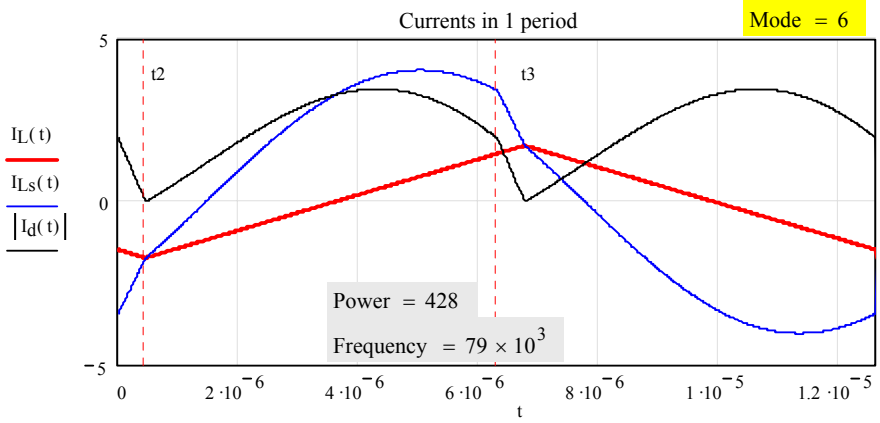


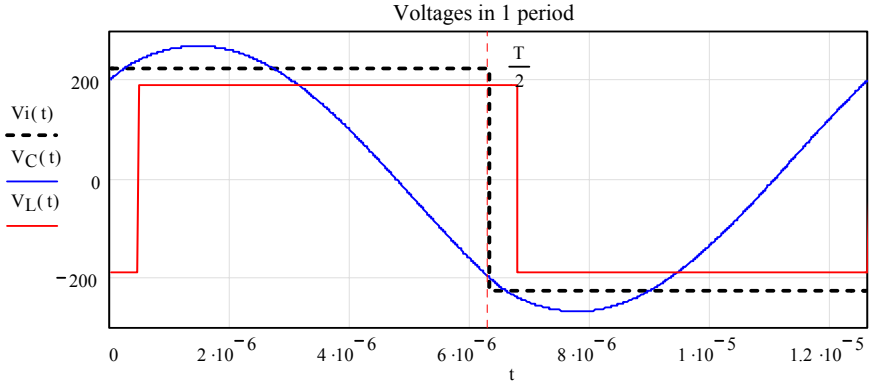
Capacitor voltage @ switching : Vc ≡ 200

Input voltage : Vin ≡ 450

When the "shoulder" in mode 5 disappears, we move into mode 6. Mode 6 looks very much like mode 5, except that there is no more dead band in diode current.

Theoretically mode 6 extends to infinity - above Vin = 2 ∗ Vo there is no power limitation.





Steady state data plots.

The worksheet cannot only calculate and plot oscilloscope waveforms of currents and voltages. It also shows a lot of data plotted against power and input voltage, which was the main purpose of creating it. It does so by running a lot of oscilloscope plots and extracting data from them.
Once you have selected a set of components and a fictitious output voltage Vo, these plots give you an overview of the converter's behaviour within a few seconds.
Here we shall see an example calculated with the following data :

Data input :

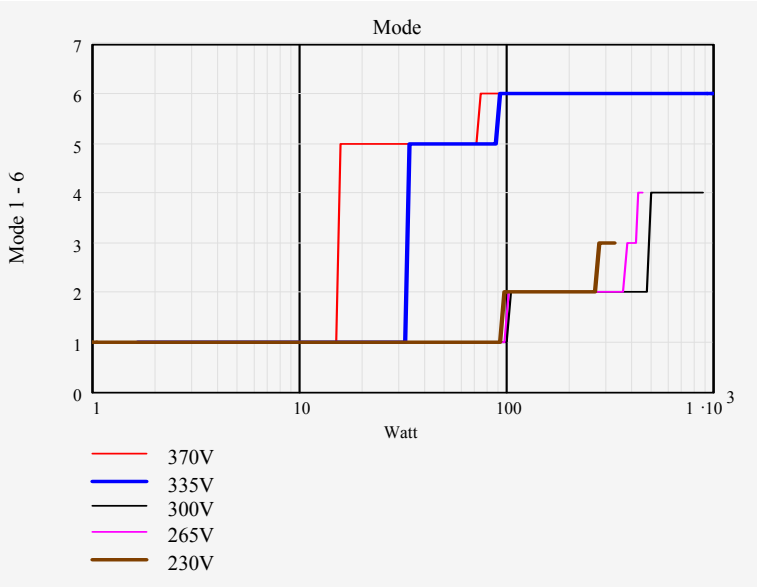
Component values :	$C \equiv 30 \cdot 10^{-9}$	$Ls \equiv 172 \cdot 10^{-6}$	$L \equiv 344 \cdot 10^{-6}$
Input voltage Vin :	$Vmin \equiv 230$	$Vmax \equiv 370$	
Fictitious output voltage in model :	$Vo \equiv 154$		
Real output voltage :	$Vout \equiv 15.7$		
Intuctance pr. turn^2 ratio :	$ALp/ALs \equiv 1$		

Turns ratio : $Np / Ns = 12.0$

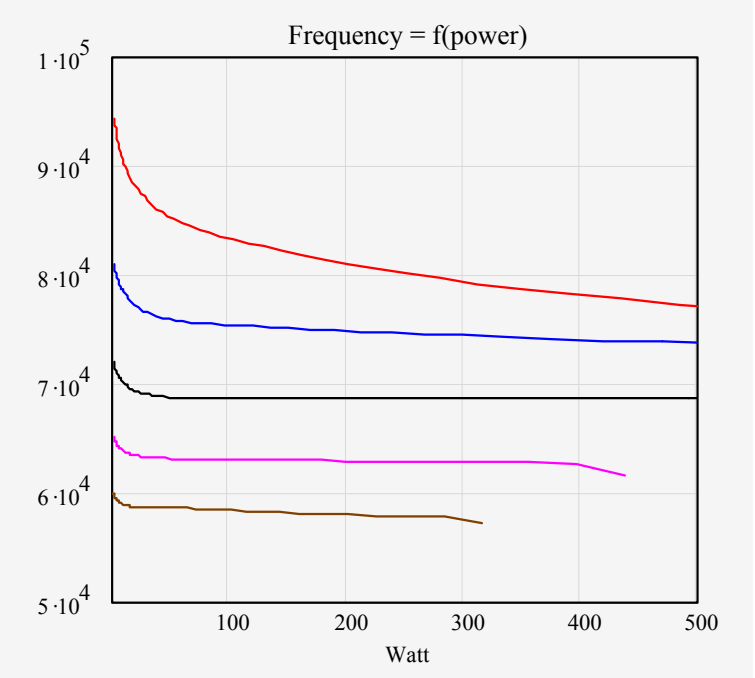
The input voltage in this example is varied in 5 steps between 230V DC and 370V DC, typical for European mains voltage rectified in a diode bridge.

To the right we see a plot of which modes are present at various power and input voltage.

Note that the lower modes below the load independent point (308V) end somewhere between 300 and 1000 Watt. The end points are the theoretical maximum powers that can be transferred.
In modes 5 and and 6 (above the load independent point) there is theoretically no power limit.



The next plot shows switching frequency plotted versus power at the same input voltages as above. The middle curve is for 300V, which is close to the load independent point 308V, and in this condition the frequency is very constant, except at low power. But also the lower curves have parts where the frequency is practically constant.
When we move significantly above the load independent point, frequency becomes more and more variable.



Calculation of rms currents.

The plots in this page show rms currents plotted against power at various input voltages.
Red is still for the highest input, and brown is for the lowest input voltage.

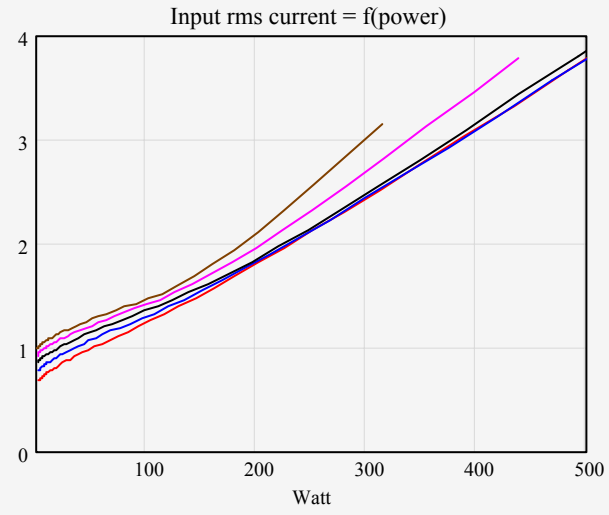
First plot is rms current in the resonance capacitor C. It is also current in the primary winding and in the input switches, and by multiplying I_{rms}^2 by the on-resistance of the switches we can easily calculate the sum of power loss in them.
This rms current poses a severe load condition to the resonance capacitor which must be a special low loss type.

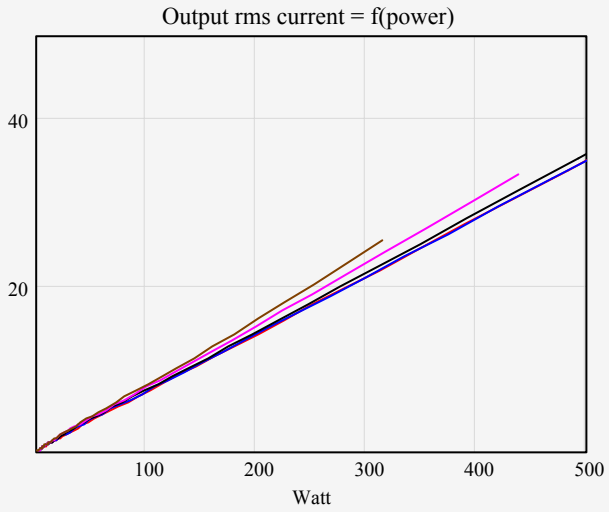
Note that there is still some current and therefore some input power loss at zero ouput power. This is due to the current flowing in the main inductor L. By increasing L the no-load loss is reduced, however the maximum possible power at low input also goes down.
The input rms current is highest at low input voltage, but the difference to higher input voltages is really not large.

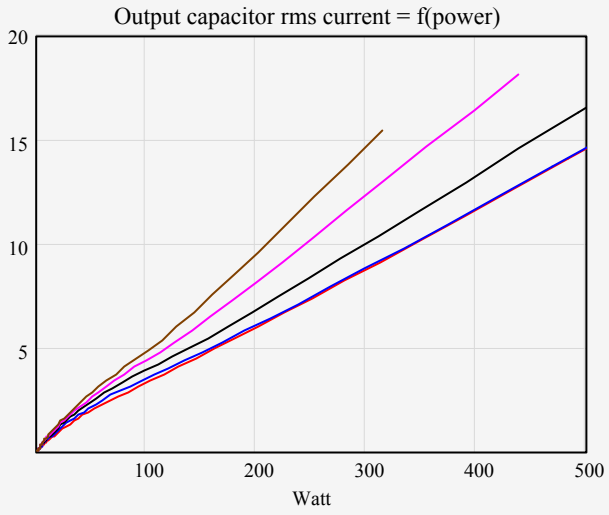
Next plot is rms current in the output winding and diodes. It is re-scaled to suit the real output voltage Vout, not the fictitious Vo.

And finally here is the rms current in the output capacitor, if the output rectifier is a diode bridge. This is also scaled to be the real capacitor current.

If desired, it will also be possible to calculate plots of e.g. peak currents at various points, but this has not been incorporated in the worksheet. Let's wait and see, if someone needs it.







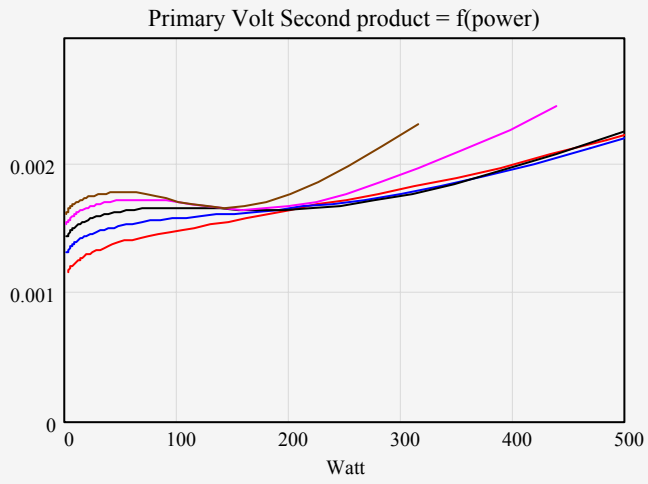
Calculation of ferrite magnetisation.

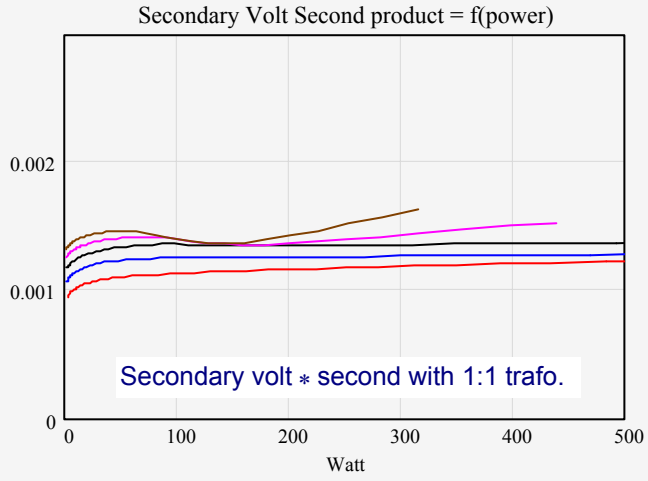
The transformer must run with safe values of core magnetisation, so that we do not risk core saturation, and so that the limits for core loss are not exceeded.
If the inductance Ls is built into the transformer as a leakage inductance, the secondary part of the transformer will have less magnetisation than the primary part.
If Ls is a separate inductor, we need to know its core magnetisation as well as the magnetisation of the transformer.

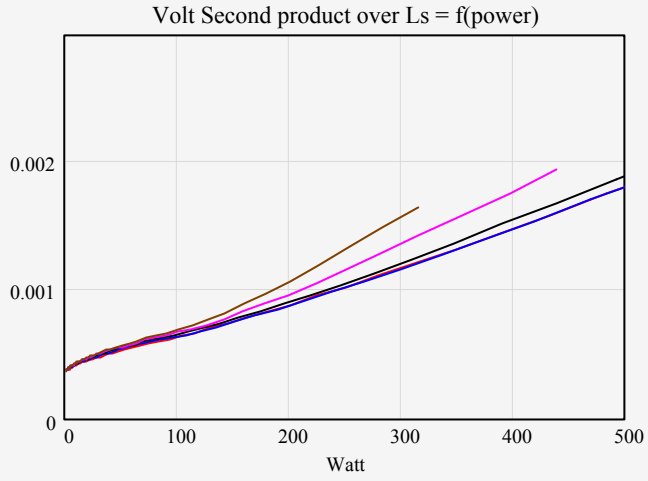
The core magnetisation follows the Volt ∗ Second product on the transformer windings according to the equation $Bpp = \frac{VS}{n \cdot A_{fe}}$ where n is number of turns and A_{fe} is the ferrite cross section area. The VS product is to be understood as the total area under the voltage curve between two zero crossings, which are separated by one half period.
Two of the three VS products can be calculated simply as the inductance multiplied by the peak-peak current excursions, which are known from the calculation of the oscilloscope plots.

The first and second plot show core magnetisation of the primary and secondary parts of the transformer respectively, if Ls is integrated in it as a leakage inductance.
In this case the core magnetisation of the secondary core part is only slightly above half of that of the primary part.
So ideally we should use a ferrite with less ferrite cross section in the secondary part to achieve a shorter secondary copper wire with less resistance.

The third plot shows core magnetisation of Ls, if Ls is a separate inductor on the primary side of a transformer with good magnetic coupling.
In that case the whole transformer will experience only the magnetisation of the 2nd. plot.







At present the worksheet can also give you an overview of core peak flux and estimated core losses for a few power ferrite types, if you select number of primary turns and data for the core geometry.
Also, if you select the wire size and number of parallel strands, power losses in the wire are calculated from the rms current graphs. The wire losses are the guaranteed losses. On top of that there will often be significant eddy current losses, if you happen to select too thick and too few parallel wires.
Some sort of litz wire is mandatory, if you integrate Ls in the transformer.

Derivation of the transformer turns ratio.

Figure 3 is identical to figure 2 but with only the relevant information. This model was used for the calculation of the oscilloscope plots. The output voltage Vo is a variable, which should be selected so as to achieve the "optimal" performance and regulation.
Usually we cannot choose the output voltage as we like. It is always given by the specification of the power supply. A transformer with uneven turns numbers can thus be used to adapt the fictitious output voltage Vo the the real output voltage Vout, however the turns ratio is NOT simply Vo/Vout. We will now find the turns ratio.

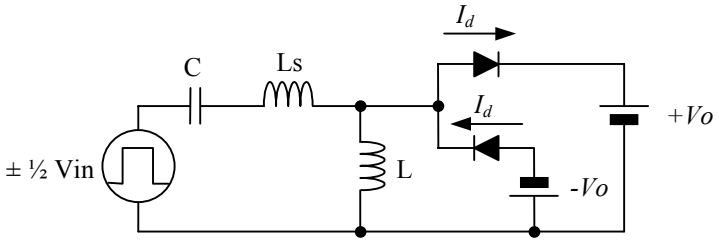


Figure 3

Figure 4 is equivalent to figure 3. We have only inserted an ideal 1:1 transformer and replaced the dual output with a single bridge rectified output.

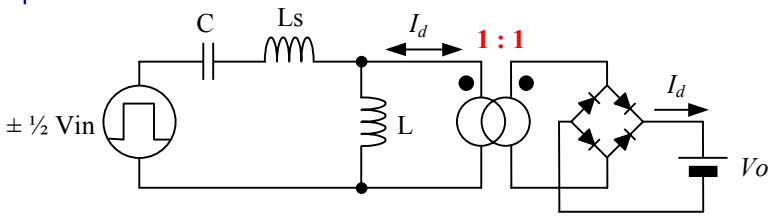


Figure 4

In figure 5 the ideal transformer is modified so that the new output voltage Vout is identical to the desired output voltage.

The voltage transformation ratio must then be $b = \frac{Vo}{Vout}$.

The circuit in the dotted area is one of the many possible models of a transformer with a finite main inductance and a non-zero leakage inductance.

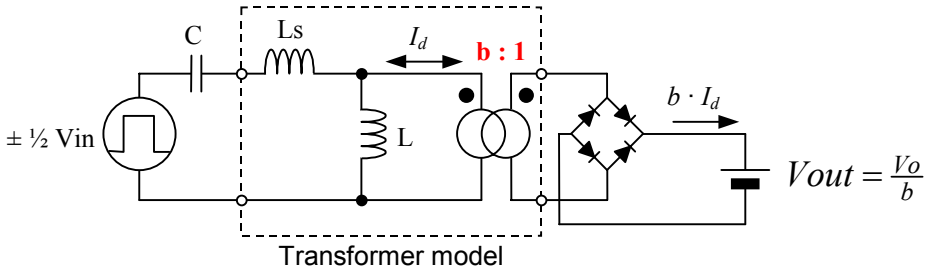


Figure 5

The transformation ratio b can be calculated like this (see also figure 6) :

$$b = k \cdot \sqrt{\frac{Lprim}{Lsec}} = k \cdot \sqrt{\frac{A_{Lp} \cdot np^2}{A_{Ls} \cdot ns^2}} = k \cdot \frac{np}{ns} \cdot \sqrt{\frac{A_{Lp}}{A_{Ls}}}$$

where k is the coupling factor : $k = \sqrt{\frac{L}{L + Ls}}$

You may have to look back in your engineering school textbooks to verify these expressions.

The turns ratio then becomes $\frac{np}{ns} = \sqrt{\frac{A_{Ls}}{A_{Lp}}} \cdot \frac{1}{k} \cdot \frac{Vo}{Vout}$

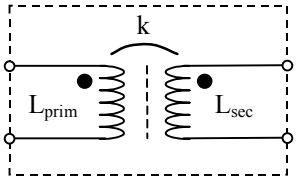


Figure 6

The real output diode current will be the calculated current I_d multiplied by b.

np and ns are numbers of turns on primary and secondary side respectively, and A_{Lp} and A_{Ls} are the core constants [Henry pr. turns²] for the primary and secondary respectively. If a spacial symmetry exists between primary and secondary, A_{Lp} and A_{Ls} are equal, so that $\frac{np}{ns} = \frac{1}{k} \cdot \frac{Vo}{Vout}$. If there is not complete symmetry (e.g. on a U-core with an airgap only in the primary leg), A_{Lp} and A_{Ls} will be different.

Scaling and adjustments.

The worksheet is a tool for analysis of a given set of component values. It can tell you how a proposed circuit will work, but it cannot give you a solution for component values based on a specification for the power supply.
It is an engineering tool, and the use of it requires some engineering skills.
Anyway I will try to give a few guidelines for using the worksheet as a design tool.

There are 4 variables which can be chosen by the user : **C, L, Ls** and **Vo** to hit a given specification. The number of possible combinations is overwhelming, so it is difficult to be sure, that we hit an "optimum" design.
If you have a first proposal of the 4 variables, and you are not satisfied with the results, you must make some adjustments. First you should be aware of two simple and obvious scaling methods : impedance scaling and frequency scaling.

Impedance scaling : If you multiply C by a number S_i and divide both inductors with S_i, then both resonance frequencies "$\frac{1}{\sqrt{L \cdot C}}$" will be unchanged, but the characteristic impedances "$\sqrt{\frac{L}{C}}$" will be S_i times lower. This means that all currents and powers will be S_i times higher for the same voltages and frequencies.

Frequency scaling : If you divide C and the two L's by a number S_f, then both resonance frequencies "$\frac{1}{\sqrt{L \cdot C}}$" will be S_f times higher, but the characteristic impedances "$\sqrt{\frac{L}{C}}$" will be unchanged. This means that you will get the same currents, voltages and powers at S_f times higher frequencies than before.

There are two more adjustment methods you will need to consider : Selection of inductor ratio L/Ls and selection of transformer turns ratio.

Selection of inductor ratio L/Ls : By having a high L (small airgap in transformer) the magnetising current is low, and since input power loss depends on magnetising current + output current, the lowest conduction losses on the input side are achieved with a high L/Ls ratio.
However for soft switching at all power levels you need a certain magnetising current. If L is too high, the primary voltage will need too long time to move to the opposite rail, when a mosfet turns off.

There are more considerations to remember :
It should be noted that when changing L (adjusting transformer airgap) the input voltage and the frequency for the load independent point stay unchanged. However with a high L, the switching frequency varies much more with input voltage, especially above the load independent point. And with a high L, zero load operation at a finite frequency is lost earlier, i.e. at a lower input voltage.
Further it appears that with large values of L, the maximum possible power is lower, when operating below the load independent point. So if you decide to increase L in order to have lower rms currents, you may have to re-adjust the L's and C for a lower impedance (impedance scaling) to re-establish the required maximum power at low Vin. Thereby some of the benefit of the higher L will be lost.

If Ls is built into the tranformer as a leakage inductance, its selection depends very much on the transformer construction. Usually Ls is obtained by physically separating primary and secondary windings. The larger separation, the fewer turns are required to give a certain Ls. A low Ls is desired, because this implies a low number of turns, i.e. low wire losses, however as the number of turns goes down the core magnetisation and core losses go up.
If Ls is a separate inductor, it should be located on the primary side, thereby the transformer will only see the secondary Volt ∗ Second product. Also in this case it is desired to have a low value of Ls to keep the component small.

Selection of transformer turns ratio : This parameter is determined by your choice of fictitious output voltage Vo. If you choose a high Vo, you can avoid operation above the load independent point. This may be desired to avoid fast turn-off of the output diodes (see time plots in mode 5 and 6). Be aware that with a high Vo there will be more magnetising current in L, i.e. conduction losses, especially at zero load, if you do not adjust L to a higher value. And if you do, you loose power capability at low Vi.
If you choose a lower Vo, you will operate below as well as above the load independent point, when input voltage varies. Usually you can then achieve lower overall rms currents and losses. You should optimise your design, so that at the lowest input voltage there is just enough power and no more.
As you let Vo go down, the diode current in the model (figure 2) must go up. This implies that also input current must go up. So if you go "too low" in Vo you will see that no-load rms currents get better, but the high-load rms currents get worse. And you soon reach the point where no-load operation is no longer possible.

In the light of the above design constraints I think it will be problematic, if someone wants to create a genuine mathematic LLC design tool where your input is a power supply specification and the output is component values. A tool like that would have to make decicions which would severely limit the user's freedom of choise and his or her insight into the way an LLC converter can work.
The design of an "optimum" LLC converter involves questions for which there exist more than one "optimum" answer. The designer has to find good compromises for the design constraints which cannot always be defined before you have gone through some of the possible solutions.

Control methods.

The LLC converter is usually controlled by frequency control, i.e. the operating frequency is derived from the output error voltage by linear amplification and filtering. This may be problematic due to the apparently infinite DC gain, as seen from the frequency plots. It will be difficult to predict open- loop gain and phase => closed loop stability and dynamic properties of the output voltage. I will assume that the small signal AC gain of the power stage must include some kind of integration, i.e. a phase shift of 90 degrees. Spice simulations indicate that : it seems to take many periods to converge to a steady state condition.
The concept of charge mode control, which was invented for the LCC resonance converter and patented by Bang & Olufsen (Patent WO2005046037A1 May 2005), is also applicable to the LLC converter, and it works just as well. It has the same attractive properties : linear, finite and predictable power stage gain with no significant phase shift. Charge mode control will even eliminate problems with unsymmetric output diode current pulses which have been seen in LLC converters.

Other LLC applications.

The LLC topology is most often chosen due to its potentially good efficiency and low EMI.
LLC will also be an obvious choice, if the converter has to transmit power through an insulating barrier, i.e. as a contactless battery charger or similar. Then the transformer inevitably must have a large airgap and a low coupling coefficient. In this case we will not be able to choose all transformer parameters. The coupling coefficient for example will be given by the physical sizes and distances between the two transformer parts.
Still the worksheet is an excellent tool to explore the possible solutions and find an optimum one.