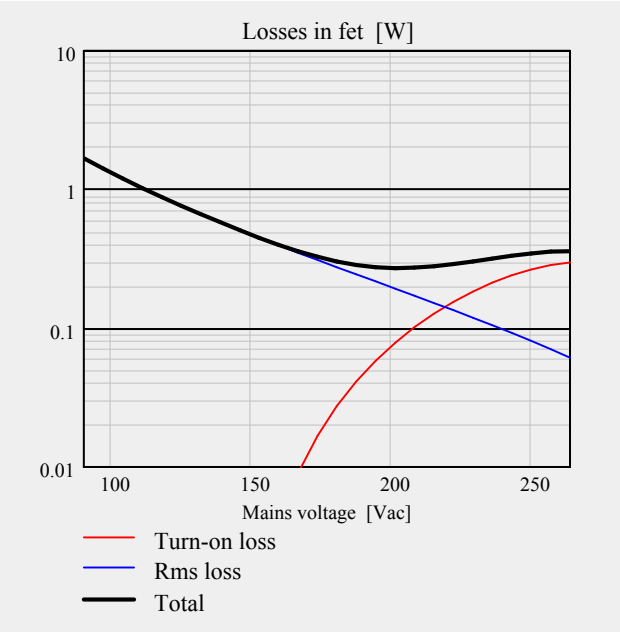
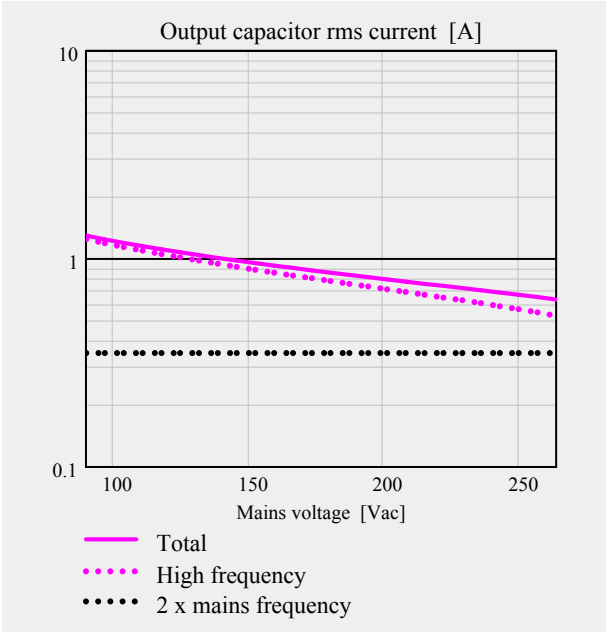
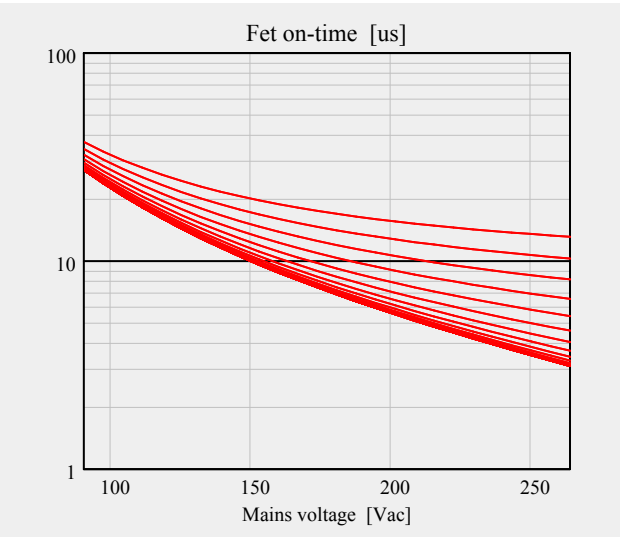
Boundary mode Power Factor Booster

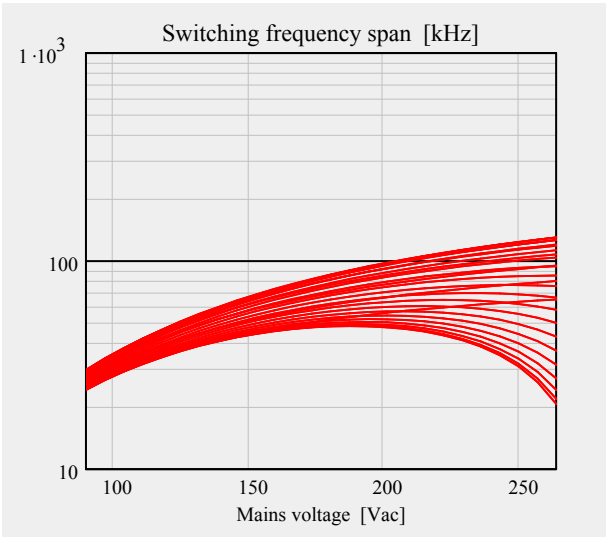
Calculation + explanation

Overview plots









Data input

Boost inductor:	$L \equiv 500 \cdot 10^{-6}$
Total capacitance in parallel with fet and inductor:	$C \equiv 400 \cdot 10^{-12}$
Fet on-resistance:	$Rfet \equiv 0.19 \cdot 1.7$
Minimum AC input voltage:	$minVac \equiv 90$
Maximum AC input voltage:	$maxVac \equiv 264$
Output voltage:	$Vo \equiv 400$
Actual power:	$POWER \equiv 200$

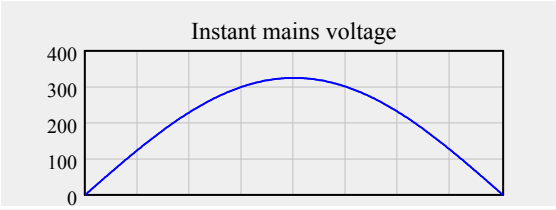
Added on-time at mains zero crossing: $\Delta Ton \equiv 10 \cdot 10^{-6}$ No correction: $\Delta Ton = 0$

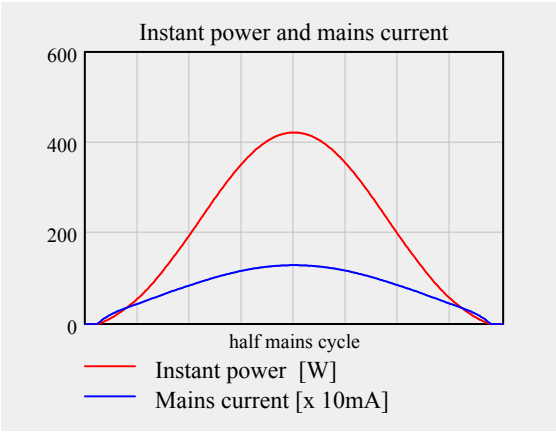
Zero crossing correction shape: $D \equiv 5$ High number => effect only close to zero crossing

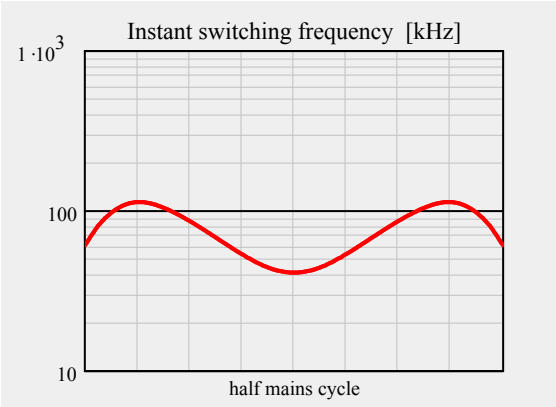
Actual AC input voltage: $V_{ac} \equiv 230$

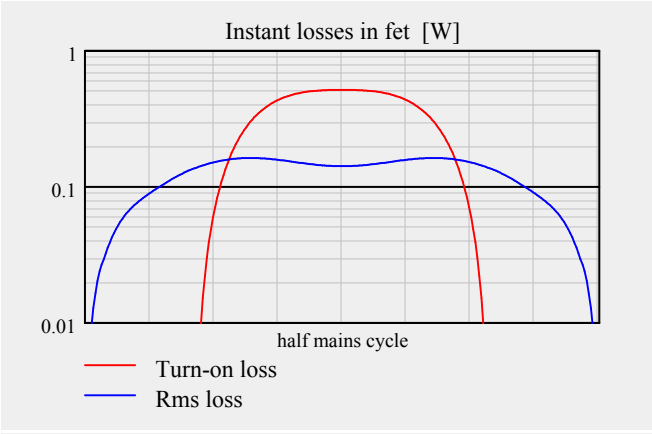
Status message:
§ = "Power OK"

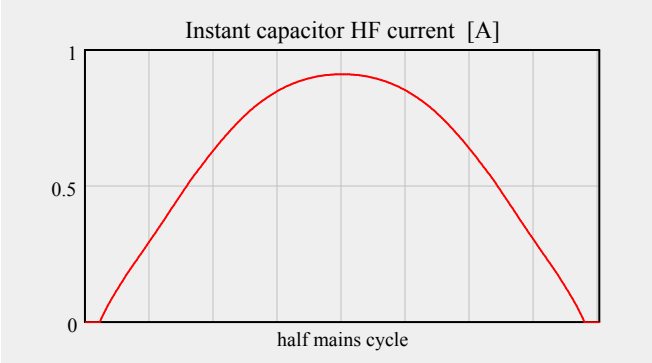
Half mains cycle plots

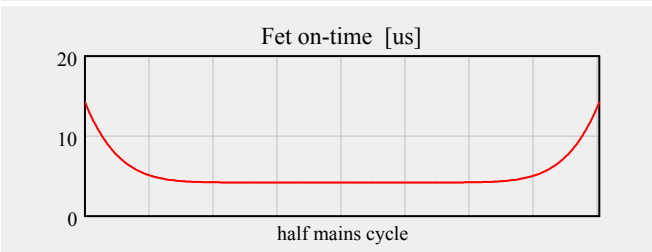


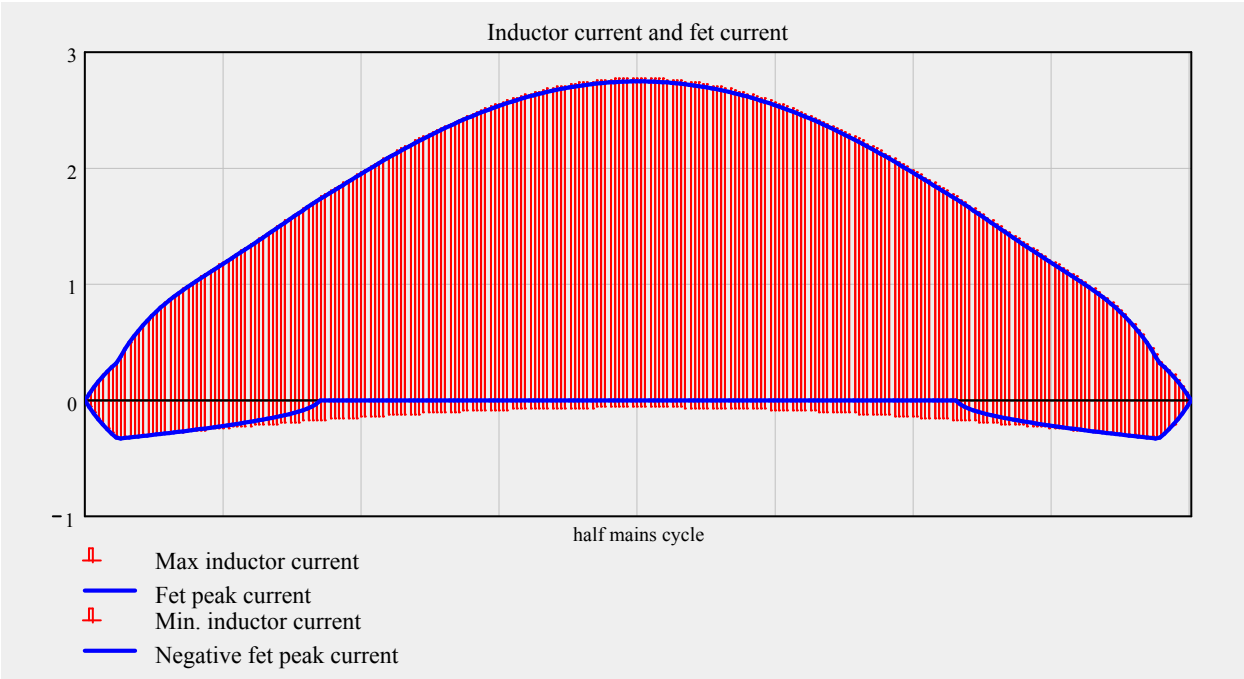












User guide

The graphs in the first page show some important variables as a function of main AC voltage, averaged over one half mains cycle.
The graphs in the second page show some variables during a mains half cycle.
The mains zero crossings are in the left and right edge of the graphs.
Input for first page is power.
You can display only one power at a time. Try with both low and high power.
Input for second page is power and mains AC voltage.

The calculations include an on-time modulation around the zero crossings to improve the zero crossing distortion inherent in the boundary mode PFC. The zero crossing distortion reduction is implemented in some PFC ICs by increasing the on-time close to the zero crossings.
A fixed extra on-time is added at the zero crossings.
You can vary the on-time modulation size and shape.

Pulse skipping at low power, implemented in some ICs, is not included.
It is assumed that the fet is turned on exactly in the first ringing valley. Or if Vi < ½Vo, exactly ½ ringing cycle after diode current stop.

At low power and high input, the on-time goes to zero, indicating that the fet must either not saturate during the on-time or skip pulses. The ends of the graphs in page 1 indicates where this happens.
Keep an eye on the status message in page 2.

Always keep the minimum switching frequency above 20kHz at max. power.

Be patient at low power and crazy waveshapes. Calculation may take many seconds.