Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Feedback in Switch Mode Power Converters

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## Introduction to feedback

Switch mode power supplies (SMPS) have been known and used for several decades. The main advantage of SMPS compared to simple linear voltage regulators with or without 50 / 60 Hz transformers are:

- There is no power loss in an SMPS – in principle at least.
- Inductive components and capacitors in an SMPS can be small and light weight because it operates at high frequency.

There are some well known drawbacks too:

- An SMPS is a noise generator which can emit electrical noise and disturb nearby electronics.
- An SMPS is complicated and not easy to design. Many things can go wrong in an SMPS, resulting in poor operation or a blown-up power supply.

One of the complexities in an SMPS is its feedback loop which will be the topic of this article.

Most SMPS must contain a feedback loop. The task of this loop is to measure the output voltage (or current), compare it to a desired value and use the error between them to adjust the switching pattern of the switch(es), until the error becomes zero or close enough to zero. Shortly explained: to keep the output voltage (or current) constant, even with a variable load, input voltage, temperature, etc. This technique is known as negative feedback, opposed to positive feedback which is used to make oscillators oscillate.

With negative feedback we want the error signal to counteract the error, with positive feedback we want it to maintain or intensify the error.

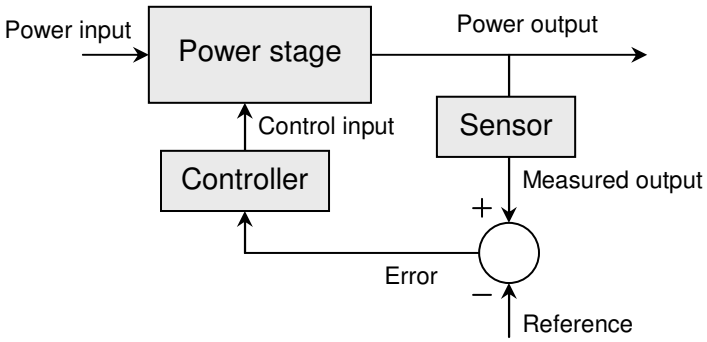



**Figure 1.** Power system with feedback

Among engineers, feedback loops are known to be normally unstable, even if they were intentionally designed with negative feedback. Self oscillation is a very usual experience for engineers who design negative feedback loops, in particular feedback loops around switch mode power supplies. The reason for this apparent contradiction is that there is no such thing as pure negative or pure positive feedback. A negative feedback system will never act with pure negative feedback at all frequencies of the error signal. The gain in the feedback path will always depend on frequency: at some high enough frequency the gain must decay and become less than one. A frequency dependent gain is always associated with more or less additional phase shift of the signal. If this additional phase shift can be 180 degrees at some frequency where the total gain in the loop is > 1 (or 0 dB), negative feedback turns into positive feedback, and the system can oscillate.

Many design engineers, when faced with an unstable feedback system, tend more or less to grope in the dark for a solution. Usually some solution to the problem is found, maybe by adding more output capacitance or adding or changing some other component by trial and error. In other cases the system happens to be stable, in which case your manager will not allow you time to investigate further whether you have a large enough stability margin, good step response etc. In both cases you may have an acceptable but rarely an optimum system. And you do not know if you are close to a stability problem or not.

Feedback loop design is really a complicated matter. The best way to deal with it theoretically is to use the Laplace transformation technique which should be known by most electrical design engineers – at least it was part of your text books at the engineering school.

Many electronics engineers are familiar with Bode plots and their linear approximation, which is a simple way to practically use the Laplace transformation. With Bode plots you can make yourself an overview of a system's so-called open loop gain and phase versus frequency by means of straight line graphs in a logarithmic coordinate system. Bode plots are (or were) usually drawn by hand, assisted by a pocket calculator. Once you have added gains and phase from all stages in a feedback system and plotted them in a Bode plot you can see if the system should be stable or not. But it is a time consuming task to get sufficient overview of a feedback system and set up a Bode plot. And only very simple systems can in practice be described in a linear Bode plot approximation.

Once you have finished your feedback loop design by means of a Bode plot, spice simulation, or whatever method you have chosen, you should always verify your result in the first prototype.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk







For many years I have used the step load test on a prototype system to test its stability. After a load step you will see an abrupt and short deviation of the output voltage from its desired value. If the voltage recovers with a ringing this is clearly an indication that the system is close to self oscillation. And if it swings back in a smooth, non-oscillating way the feedback system is good and has a good margin to instability. Well - in most cases this is true. But after learning how to calculate feedback loops, I found that there are exceptions to both statements. For instance you can have a nice step load response, but if you increase your error amplifier gain just 3dB your system can oscillate. So a nice step load on your scope is not always a guarantee. This came as a surprise to me after having worked with SMPS for more than 20 years.

An experienced SMPS designer also knows that although a proper gain and phase design is required, there are other ways an SMPS can become unstable. Often such kinds of instability are caused by unwanted noise signals intruding into your feedback path or by non-ideal waveshapes in your power stage.
If your system seems to be unstable it is therefore important that you can distinguish between feedback loop problems and noise and distortion problems. If you have designed and calculated a stable SMPS – and if you trust your calculations – you know what kind of instability you are dealing with.

For these reasons, the ability to theoretically calculate and optimize your feedback loop is essential. You are supposed to be efficient in your work, so your calculator must be detailed enough, easy to use, and fast. If it could also give you a general insight into regulation issues of switch mode power supplies, it would be great.

It is my conviction that a deep (enough) insight into technical matters is the creator of good engineers and good engineering. There are numerous sites on the internet offering design help, enabling you to design your power supply without really knowing much about it. In many cases this is good enough, but relying only on calculators where all the difficult stuff is hidden in inaccessible and unverifiable code, does certainly not make the best engineers.

## General SMPS case – a historical retrospect

Figure 2 is an example of a switching power supply comprising a generic power stage, a voltage reference, an error amplifier and a pulse width modulator (PWM) stage. In case of a galvanic separation between input and output, some insulating device like an opto coupler must also be part of the feedback path.

The power stage and the Pulse Width Modulator (PWM) are the difficult parts in the feedback loop analysis. Other parts like error amplifier, opto coupler, and additional active or passive filters can be easily described by Laplace transfer functions. The difficulty arises when trying to describe small signal AC transfer functions of the power stage and the PWM.

In the 1970's Dr. R. David Middlebrook developed a technique called "state space averaging" – a way to describe and calculate the frequency dependent gain of an SMPS power stage. This technique is often quoted and extended in later literature and courses about this subject. In articles, that I have seen, the state space averaging very soon evolves into an advanced form of matrix math, which is unfamiliar to many SMPS designers, including me. As a result, although the contents are very simple looking expressions, the reader or listener is "disconnected" and has little chance to follow the genius and basic rules of the loop calculation technique, and thus to use the information to create his or her own loop calculator.

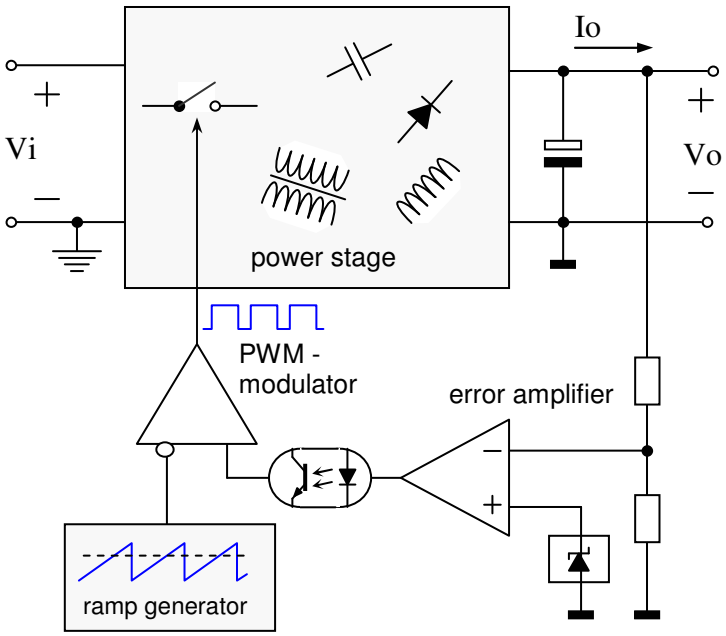



**Figure 2**

In 1989 Mr. Vatché Vorpérian introduced the PWM switch model (ref. 13) which is a three-terminal model of the two switches (normally a fet + a diode) in a pulse width modulated converter. In some respects, this model simplified the modelling of feedback loops and shows special benefits when using it in combination with simulation software like Spice. Still, the PWM switch model can appear quite abstract and difficult to comprehend for many practical SMPS designers.

Using matrix math or PWM switch model is not paramount for SMPS loop analysis, although I believe matrix math does yield simple looking closed form solutions, suitable for computer calculus. What is really important for both concepts is that they deal with **average values of currents and voltages during each switching cycle**. Using averaging or using the PWM switch model, all information on switching waveforms is lost. This can be justified for the feedback loop which by nature deals with “low” frequencies. Output signals are assumed to be DC, on which deviations are of low frequency nature compared to the switching frequency. Switching frequency ripple must be filtered out in the loop to fulfil the basic ideas of feedback and regulation.

## Feedback loop calculators

During my years as an independent SMPS designer I have developed a handful of Mathcad worksheets for calculation of feedback loops in various topologies, containing a lot of useful and some never before seen features. In my own work they have proved extremely useful.
We will see some of these features in the next pages.

The reason for writing this article is to promote my SMPS loop calculators for the SMPS world.

All of the worksheets are based on quite elementary high school math, without using matrix math or other advanced mathematical abstractions. This basic math level suits my own skills and education level, and I am sure many of my colleagues out there will see it the same way.

But don’t be mistaken. You will be amazed by what you can do with elementary high school math.

However, Laplace equations based on the complex frequency “s” are used again and again. Fortunately, I think Laplace transformation is known by most electronic engineers.

Mainly for my own memory, I have also documented my worksheets in a little electronic text book in which you will find detailed explanations on how all my equations were derived. Many of the equations that I used are the solutions to a sequence of several equations with several unknowns, and without some documentation they are literally impossible to check, let alone remember.
The text also contains lots of “side effect” knowledge, which was very educational for me to discover.

I am planning to offer this e-book for the SMPS public together with my loop calculator worksheets. My aim is to make my work useful to all of you who struggle with SMPS loops and stability.

But especially, I would like to offer tools with built-in self education. It is becoming still more evident to me that our world needs educational tools enabling engineers to look behind the curtain and understand things, more than just tools which blindly provide results fast. Therefore I will not follow the more usual track of hiding difficult matters in invisible and unverifiable code, as done by many on-line design tools and some design software for purchase.

I would like to show you that theoretical engineering does not have to be inaccessible black magic, as you probably thought.

My tools will be open source, so those of you who feel like it, can use them for inspiration to create your own tailor made worksheets for your specific needs.

But before we start to discuss SMPS feedback loop properties , let us have a short revision of some basic concepts.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



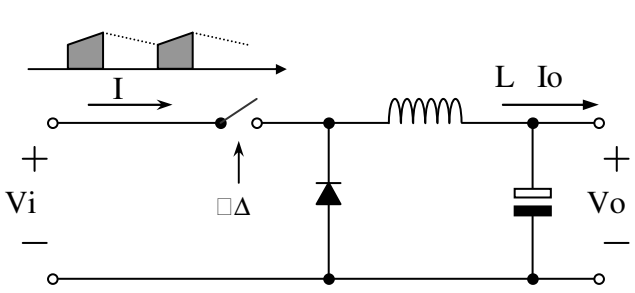




# Basic pulse width modulated topologies

The power stage of most SMPS converters used today are variants and extensions of one of the three basic topologies: **buck** (step down), **boost** (step up) and **buck-boost** (step down+up). The next figures show the three basic topologies with their steady state transfer functions (in continuous current mode, i.e. if current is so high that inductor current never hits zero). Δ is duty cycle.

The heart of each of these three topologies contains one active switch, one diode and one inductor. Small signal gain properties of the buck can easily be extended for use in most buck-derived converters. The same applies to boost and buck-boost. So it is important to understand the power stage transfer functions of these three topologies.



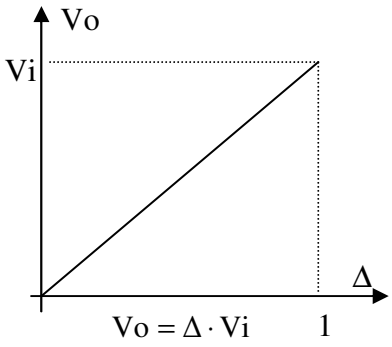
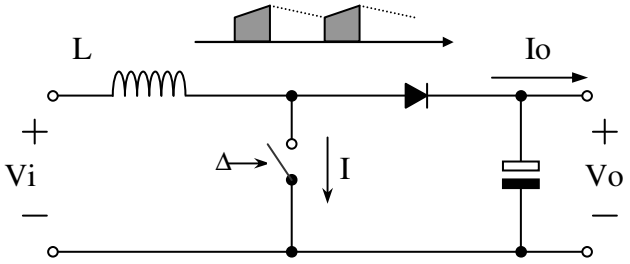




**Figure 3** Buck converter



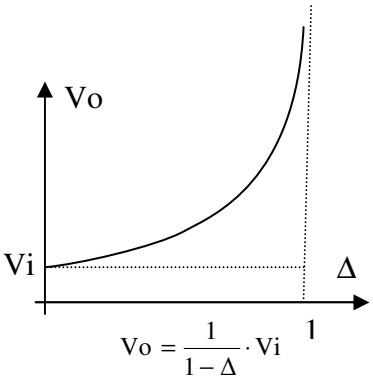
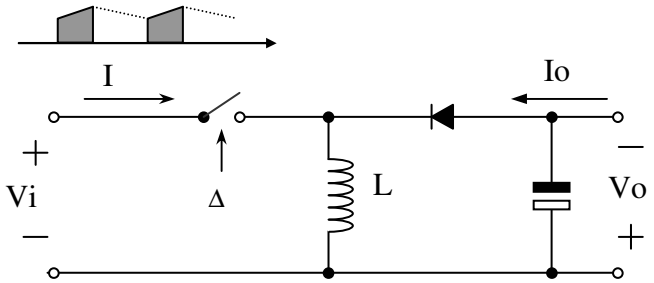




**Figure 4** Boost converter



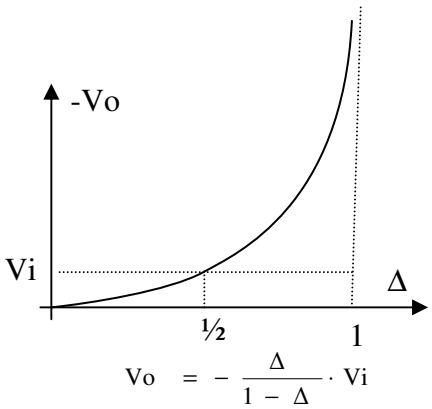




**Figure 5** Buck-boost converter

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk







# Control methods in pulse width modulated converters

Let us also talk a little about basic control methods of pulse width modulated converters.
The active switch is turned on and off at a fixed (high) frequency, and the pulse width – or the duty cycle – of the switch's on-time is controlled by a feedback signal which is derived by linear amplification and filtering of the error signal (error = difference between actual output voltage and desired output voltage). If, for some reason, the output voltage is lower than desired, the duty cycle must be adjusted up, to get the output voltage back on the desired value.
The oldest control method is known as "Voltage Mode Control" (VMC). With VMC, the pulse width is determined by comparing the slowly varying feedback signal to a fixed modulator ramp, as illustrated in figure 6.

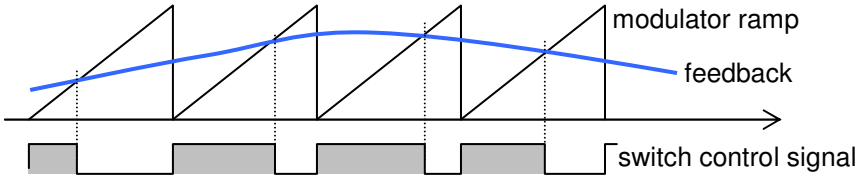



**Figure 6** Voltage mode control

In my opinion, voltage mode control is a misleading name. I would rather like to name it "pulse width control" or "duty cycle control", since the controlled parameter is the pulse width or duty cycle of the active switch.

Around 1975 a new control method called "Current Mode Control" (CMC) started to be used in pulse width modulated converters, and since then it has become still more popular. The switch is turned on by a clock signal and turned off when the current in the inductor or the switch reaches a value determined by the feedback signal. This is shown in figure 7.

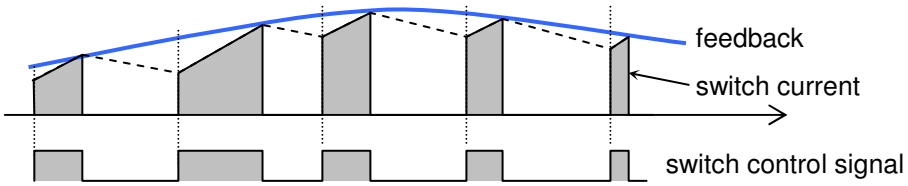



**Figure 7** Current mode control

In CMC the control parameter is not pulse width but peak current in the inductor. That means that the control circuit in principle does not know and does not care about pulse width, although of course the pulse width always does have a value.

Today, many power supply designers prefer CMC over VMC due to the following advantages:

1. A power stage with VMC has two complex poles. A power stage with CMC has only one real pole. This makes it simpler to close the feedback loop with CMC and most often with better results.
2. CMC has an inherent current limiter since current is measured and controlled from pulse to pulse.
3. CMC does not show the abrupt change in power stage gain on the boundary to discontinuous current as VMC does.

However, a disadvantage with CMC is that it becomes unstable when the duty cycle is above 50%. This instability, called subharmonic oscillation, has nothing to do with the outer feedback loop. It is inherent in the current mode controller itself (ref. 1 + 2 + many others).

The normal way to prevent subharmonic oscillation is to add a ramp signal, typically a fraction of the oscillator ramp, to the current signal, before comparing it to the feedback signal. This technique is often referred to as "slope compensation". It is important to note that CMC with slope compensation is really a combination of pure VMC and pure CMC, so the more slope compensation you use, the more you lose the mentioned three benefits of CMC. Too little ramp does not prevent subharmonic instability. More ramp than necessary can still work fine. But with slope compensation, a high frequency pole returns into the power stage gain, current limit becomes less accurate, and loop gain again experiences an abrupt change on the boundary to discontinuous current mode.
Voltage mode and current mode control can be used in all three basic topologies: buck, boost, and buck-boost and their derived topologies, except in the half bridge where current mode control has problems (ref. 12).

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



## What you really need to calculate

In texts on SMPS feedback loops you are usually taught how to calculate OPEN loop gain and phase. It is indeed very essential to do this in order to assure stability of any feedback system. The concept of designing open loop gain and phase for good stability is well known. A rule of thumb, for instance, teaches us to design for a phase margin of at least 45 degrees which means that the phase delay must be maximum 135 degrees at the frequency at which the TOTAL open loop gain magnitude is 0 dB. Also, a certain gain margin is necessary: a good rule of thumb is to keep open loop gain magnitude at maximum -10 to -6dB ( |gain| < 0,3 to 0,5 ) at the frequency at which the phase delay is 180 degrees (= positive feedback). Doing so will assure stability, even with some variation in circuit parameters. Usually it also assures a reasonable, non-ringing response to load steps.

But you cannot tell much about how the output voltage will swing as a result of a load change or how fast or how well it will return to its nominal value. In some power supply designs, this kind of performance data is part of the requirement specification. It can be specified as a maximum allowed output impedance in a certain frequency range, or as a maximum voltage jump and max. recovery time after a load step from 10 to 90% of full load – just to mention a few ways to specify it.

In order to handle this kind of design data we need to be able to calculate output impedance of a power supply versus frequency when the feedback loop is CLOSED, i.e. how the output voltage is affected by load current perturbations.

Texts on SMPS feedback design usually do not go into this area, which is very strange because what really matters are the properties of the CLOSED feedback loop: how stable is the output voltage (or current) and how does it react to a sudden load variation?

In many switching power supplies a very clean (ripple free) output voltage is required. Especially the boost and the buck-boost + flyback converters are known for high ripple current in the output capacitor, and the most efficient way to suppress ripple is often to add an LC filter to the output. To be effective, the resonance frequency of this filter must be much less than the switching frequency, which means the resonance moves down close to the frequencies handled by the feedback loop. If insufficiently damped, this resonance can create huge trouble and self oscillation close to the filter's resonance frequency. No text book or calculation software that I have seen deal with this real-life-problem.
Having inserted the LC output filter, you also should know the consequence of connecting your feedback point before or after the filter – which point is best? Or should we connect it to a point "in between"?
Further, in many real cases you have two inputs for your error amplifier (but you may not be aware of the second input). Then you have even more options of where to connect which input. The possibilities seem overwhelming but don't despair – it can be easily handled and the results can be viewed and evaluated at a glance.

And wouldn't it be nice if we could calculate the scope picture of for instance a step load? A calculated scope picture will show the expected peak voltage deviation, permanent voltage deviation, settling time, wave shape, ringing etc. And you will be able to compare it to a real step load response on your oscilloscope. If they fit, you can leave your network analyzer (if you have one) on the shelf and use your calculated open loop data for your documentation. It can save time for you and even give you more useful information about your power supply.

All the described features are included in my mathcad tools.

For PWM modulated converters, the tools also detect whether you are in continuous current or discontinuous current mode and show you the results accordingly. You can apply Voltage Mode Control or Current Mode Control with or without slope compensation. And when you hit "F9", you have results in fractions of a second.

## Difference between topologies

It would be nice, if the control rules for the buck power stage could also be applied to the boost and the buck-boost converters. After all, they contain the same elements: switch, diode and inductor.

Unfortunately they can't.

The simplest of the three seems to be the buck converter, which is also the topology having the most attractive gain properties. There is no sampling delay associated with the buck power stage (more about that later) as in the two others. The buck power stage gain does not depend on transfer ratio or power – for boost and buck-boost it does. And the buck does not possess the notorious "**R**ight **H**alf **P**lane **Z**ero", as the boost and the buck-boost do.

Most presentations of loop theory start with the buck converter. Some of them even do not go further. In my opinion the basic buck converter is "too simple", and some results seem to be obvious – they can be derived by pure inspection of the circuit. The boost and the buck-boost are less intuitive, as we shall see.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk







## Buck converter

The buck – or step-down – converter is one of the most used topologies in the world, including all the many buck derived converters. Its loop characteristics with Voltage Mode Control (duty cycle control) and continuous current can be understood simply by inspection of the circuit. Assuming ideal switch and diode (no voltage drop), the voltage Vs after the switch has average value $Vs = \Delta \cdot Vi$ and since there can be no DC voltage drop over an inductor, $Vo = \Delta \cdot Vi$.
A load current generator Io is implied but not shown.

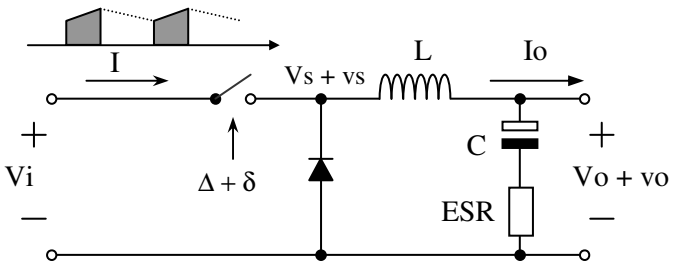



**Figure 8** Buck converter

If the duty cycle is modulated with small signal δ(s), the small signal input voltage component will be $vs(s) = \delta(s) \cdot Vi$ and the output small signal voltage, by simple voltage division, will be

$$vo(s) = \delta(s) \cdot Vi \cdot \frac{\frac{1}{sC} + ESR}{sL + \frac{1}{sC} + ESR} = \delta(s) \cdot Vi \cdot \frac{sC \cdot ESR + 1}{s^2 LC + sC \cdot ESR + 1} = \delta(s) \cdot Vi \cdot \frac{ESR}{L} \cdot \frac{s + \frac{1}{ESR \cdot C}}{s^2 + s \cdot \frac{ESR}{L} + \frac{1}{L \cdot C}} \equiv \delta(s) \cdot Vi \cdot \frac{ESR}{L} \cdot \frac{s + zero}{s^2 + s \cdot d \cdot \omega_o + \omega_o^2}$$

so the gain of the buck stage is $$\frac{vo(s)}{\delta(s)} = Vi \cdot \frac{ESR}{L} \cdot \frac{s + zero}{s^2 + s \cdot d \cdot \omega_o + \omega_o^2}$$

with the well known resonance frequency and damping factor etc.:

$$f_o = \frac{\omega_o}{2\pi} = \frac{1}{2\pi\sqrt{L \cdot C}} \qquad d = \frac{ESR}{\sqrt{\frac{L}{C}}} \qquad zero = \frac{1}{ESR \cdot C}$$

The gain vo/δ versus frequency is plotted in figure 9 for
$Vi = 10V,\ L = 100\mu H,\ C = 100\mu F,\ ESR = 0{,}1\Omega$.

The resonance frequency is fixed, and the gain from duty cycle to output voltage is proportional to input voltage.

The DC gain of 20dB is simply the input voltage 10V: when Δ varies from 0 to 1, the output voltage will vary from 0 to 10V.

At the resonance frequency the phase suddenly swings from zero to -180 degrees. However, the effect of the ESR in the output capacitor is to increase gain and reduce phase lag at high frequencies back to -90 degrees. Since the regulation bandwidth of a feedback loop is normally > fo, the ESR or lack of ESR will have enormous influence on loop stability. A very low ESR (good capacitor) can lead to a too low phase margin, causing ringings, a high ESR (bad or cold electrolytic capacitor) can boost the high frequency gain to cause high frequency oscillation.

The 2nd order property of the power stage gain is undesirable, especially for capacitors without ESR (ceramic capacitors). To compensate for the 180 degrees phase lag it is necessary to use a so-called “type 3 compensator” around the error amplifier which introduces an “ESR” effect in a limited frequency range. But it can result in a delicate design which is not very tolerant to circuit variations.

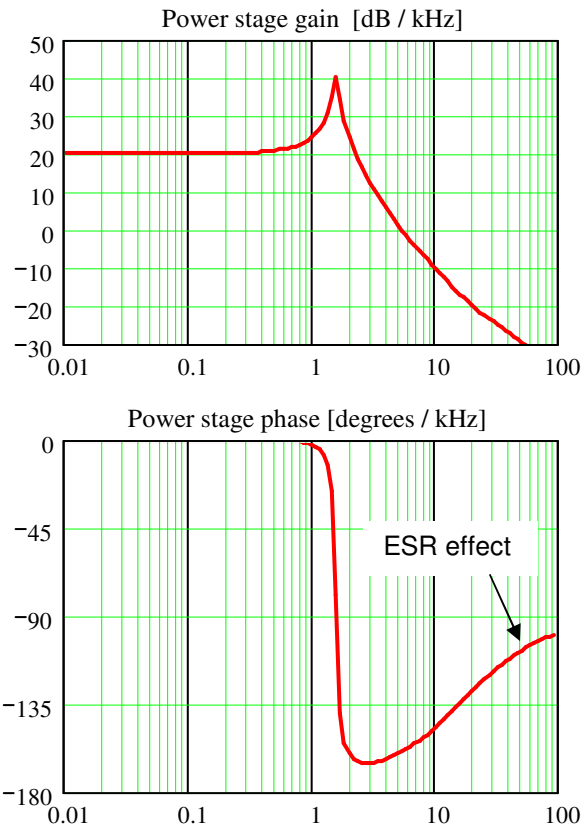



**Figure 9**
Open loop gain of a buck with VMC

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk







# Closing the buck feedback loop.

Here is the same buck regulator with input = 30V and 10V output.
The control method is Voltage Mode Control. This error amplifier is assumed to be ideal and have infinite bandwidth. The modulator gain of 1/V means that duty cycle varies from 0 to 1 when the error amplifier output moves +1volt.

Below, you see the calculated TOTAL open loop gain and phase, including the voltage divider and error amplifier. This error amplifier is a "PI" (proportional + integrator) amplifier. More components can be added around the error amplifier to change its frequency characteristics.

We can still see the LC resonance at 1.5kHz. Here it is a little more damped by the load resistance of 10Ω.

The lowest graph shows the output impedance magnitude of this buck converter (as long as it is in continuous current mode !!). At low frequencies, where the error amplifier's integrator effect is active, the |Zo| drops with 40dB/decade.

You should notice that the LC resonance becomes completely invisible in the closed loop properties. This would be true even with an infinite LC peaking. This fact seems in deep contradiction with human intuition, at least with mine. The peaking in the closed loop graph – if any - will be at another frequency: where the open loop gain goes through 0dB. This peaking will be high if the phase margin is low, i.e. if the phase graph is too close to the -180 degrees line at the 0dB frequency. In this example there is a phase margin of exactly 45 degrees which is normally considered the minimal acceptable but still good stability margin.

This converter shows a good example of what is known as "conditional stability". The converter is completely stable and regulates well but if, somehow, the gain is reduced 30dB, it will oscillate at 3kHz because phase margin at that frequency is zero degrees.

The fact that it cannot oscillate with a phase shift of 180 degrees if the open loop gain is still high at that frequency is another punch to what we thought we knew. Most of us would say that if a system oscillates at some loop gain, it would oscillate more violently if loop gain is increased. But no – in this example we are wrong!

Just a note on load resistance.
Most literature on loop stability lets Rload be = Vo/Io, where Io is the DC load current. This is true of course if the load is a real resistor. But the load of an SMPS can be anything, so it is wise to set Rload close to ∞ to simulate a true current load. Any peaking will be damped less if you do that. The dynamic load resistance can even be negative if the load is another SMPS, in which case funny things can happen.

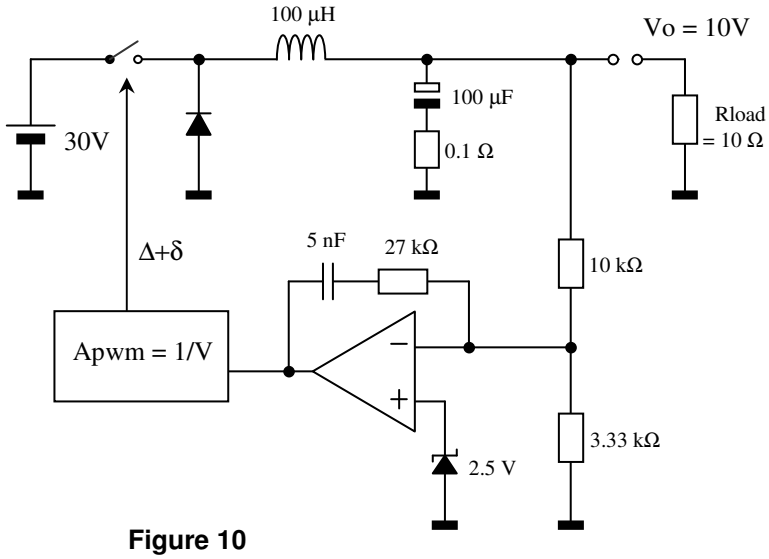



**Figure 10**
Complete buck converter with feedback loop

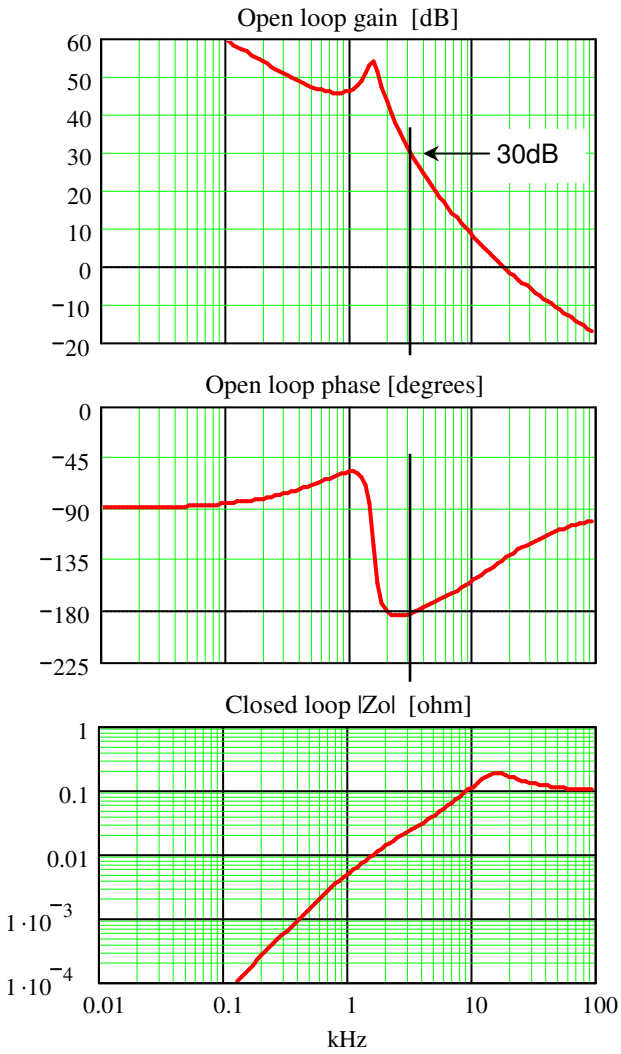



**Figure 11**.
Buck converter open and closed loop

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Feedback in Switch Mode Power Converters



Going a step further, here is a calculated step load response for the same buck converter. There is a clear but strongly damped ringing. The ringing frequency is not the LC resonance frequency – again that frequency has apparently vanished, although it must still be alive inside the converter.

This calculated result can be easily checked with an oscilloscope and a step load generator. If it fits in magnitude and shape, you know that your open loop calculations are 99% likely to be correct. Having done the calculation, you even know much more about your circuit than you would know by measuring open loop gain and phase with a network analyzer.

A phase margin of 45 degrees is some times believed to give an exponential-like and non-ringing step load response. Well, some times it does, some times it does not. In this case, not at all. So you cannot describe the stability of a system in terms of phase margin by just observing the step load response on your oscilloscope.

**Test frequency:** Fo ≡ 2000 [Hz]

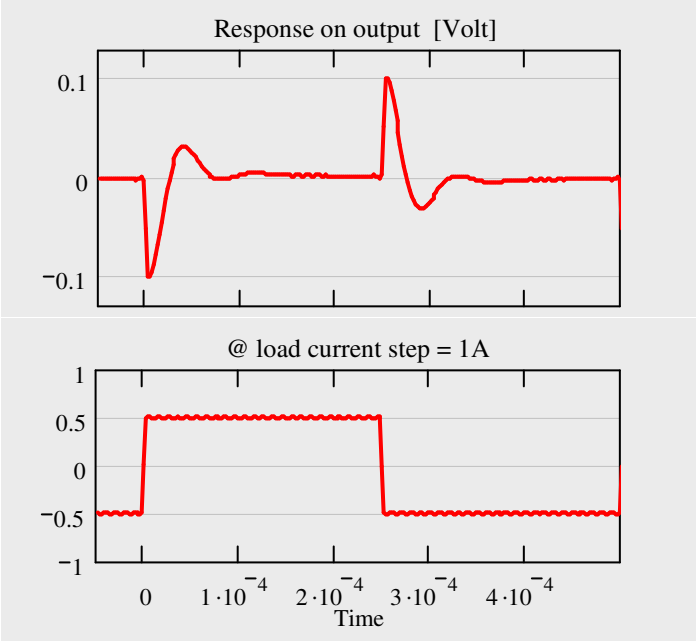



**Figure 12.**
Step load response with closed loop

For many years, before I did the math studies, I used the step load test to verify and adjust my feedback loops, which is in 95% of all cases a fast and good way to do it. But there may be cases in which you have a gain margin of only 3 dB and still a very nice and fast step load response. Increasing gain just 3 dB in such a case will make the converter oscillate – this could easily happen by cooling down the output electrolytic capacitor, i.e. increasing its ESR. I learned that by playing with my math tools and also verified these surprising results by real experiments in the early days of the tools.

## Boost converter

The boost or step-up converter is shown in figure 13. The gain of the boost stage cannot be found just by inspection of the circuit diagram, like the gain of the buck. A study of the interrelation between incremental (lower case) voltages, currents and duty cycle in figure 13 leads to the following expression, containing resonance frequency, damping factor etc. (Rload is set to infinity here):

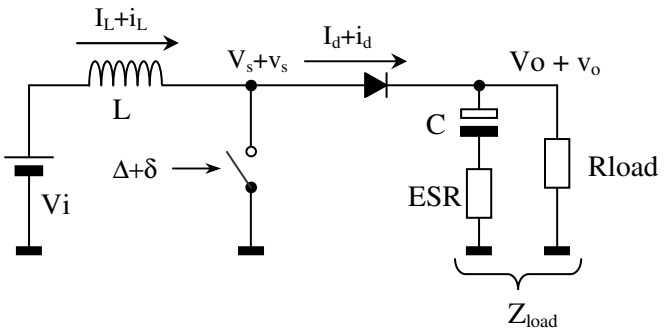



**Figure 13.** Boost converter

$$\frac{vo(s)}{\delta(s)} = (-I_L)\cdot ESR\cdot\frac{(s-RHPZ)\cdot(s+zero)}{s^2+s\cdot d\cdot\omega_o+\omega_o^2}$$

where

$$f_o = \frac{\omega_o}{2\pi} = \frac{Vi}{Vo}\cdot\frac{1}{2\pi\sqrt{L\cdot C}} \qquad d = \frac{Vi}{Vo}\cdot\frac{ESR}{\sqrt{\frac{L}{C}}} \qquad RHPZ = \frac{Vi}{L\cdot I_L} = \frac{Vi^2}{L\cdot P} \qquad zero = \frac{1}{ESR\cdot C}$$

These equations are valid for Voltage Mode Control and in Continuous Current Mode.

There are several interesting things to note.
Like in the buck, there is a resonance frequency $f_o$ but this one moves with step-up ratio. So does the damping factor $d$.
The zero is the same as in the buck, given by the output capacitor with its ESR.
But this numerator also contains a Right Half Plane Zero RHPZ, characterized by the minus sign in front. For this factor to become zero, $s$ must be a positive number, which is opposite to usual zeroes.

Derivation of these equations can be found in my e-book.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Feedback in Switch Mode Power Converters



If we insert the four terms in the equation for $vo(s)/\delta(s)$ and set $s = 0$ (DC), we get an expression for the non-linear slope of the curve in figure 4: $\frac{vo}{\delta} = Vi \cdot \left(\frac{Vo}{Vi}\right)^2$

indicating that the slope grows with step-up ratio squared. But this is just foolish playing around with the equations – the last equation could be obtained much simpler by differentiating the boost steady state equation in figure 4 (find $dVo/d\Delta$ and do a few substitutions).

The Right Half Plane Zero can be very unpleasant in a feedback loop, since its effect is to increase gain, accompanied by an additional phase *lag*, which is opposite to a "normal" left half plane zero.

This behaviour is illustrated in figure 14. In the time domain its effect is to start moving the output (diode) current the wrong way when the duty cycle changes suddenly, as seen in figure 15. If, for instance, the duty cycle takes a positive step, the diode conduction duty cycle takes a negative step, so that the average diode current steps down, until inductor current ramps up after some time. It is evident why this behaviour causes trouble in a feedback loop, most trouble if the inductor current response time is high.

The equation shows that the RHPZ is lowest (worst) at low input voltage, high power, and a high inductor value. The RHPZ puts a severe limit on how ripple-free a booster's input current can be if you need a reasonably fast responding system.

The RHPZ is also present in the buck-boost and flyback converters in continuous current mode and some others, but not in the buck or (most) buck derived converters.

The RHPZ is interesting not only in academic discussions. It will make your system unstable before you imagine so you should really know where it is.

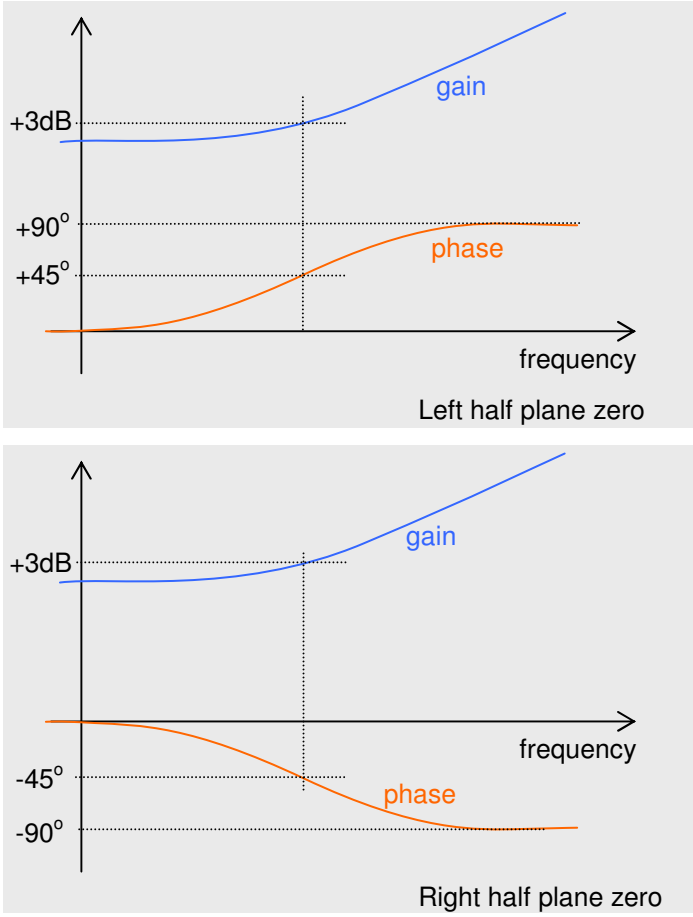



**Figure 14**

## Buck-boost converter

The buck-boost converter's regulation properties are very much like those of the boost converter. The boost and the buck-boost can be considered basically the same converter – the difference is the return point of the output. In the buck-boost the return point is not ground as shown in figure 13 but the +side of the input battery. If both are considered DC points, the small signal equations will be similar.

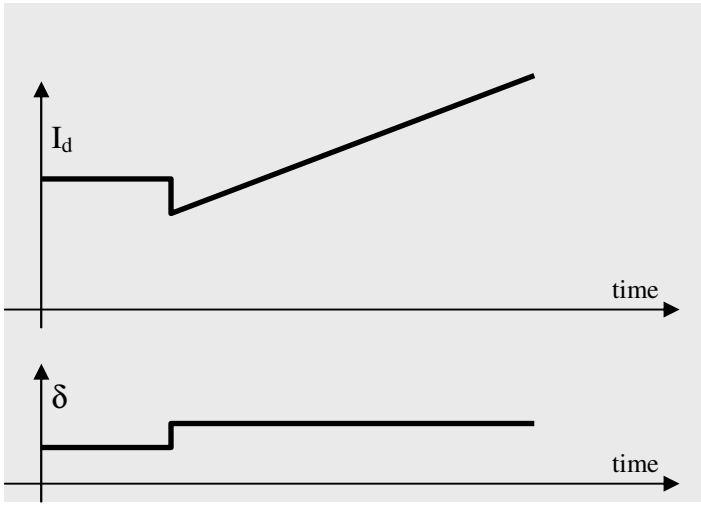



**Figure 15.** Effect of the RHPZ

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Current Mode Control

The discussion in the previous pages has only dealt with Voltage Mode Control. Today, Current Mode Control, as explained in page 5, is perhaps more popular due to its attractive properties. However, CMC requires to measure the current in the inductor or in the switch with some kind of fast current transducer. The simplest current transducer is a resistor.

We also know that CMC at duty cycles > 50% requires us to add a ramp to the measured current to avoid subharmonic oscillation. A model for the pulse width modulator in a CMC system is shown in figure 16. Now the control variable is the control voltage $v_g$. The duty cycle is still present in the system but it is not a directly controlled parameter any more.

Looking at figure 16, obviously the duty cycle depends on $Vg$ as well as $Vsens$, since both are inputs to the comparator which determines $\Delta$. In other words, $\delta$ is a function of both the control variable $v_g$ and the peak current $\hat{i}_L$.

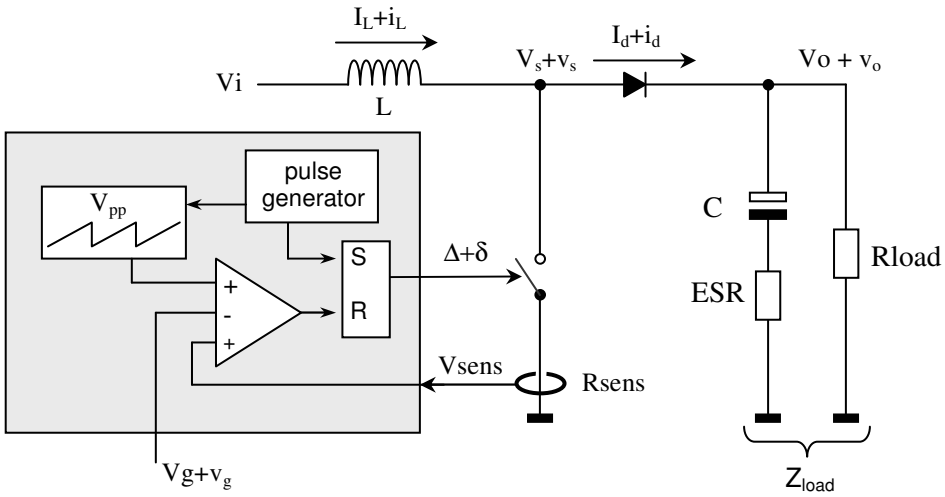



**Figure 16.** CMC modulator model in a booster

Below, I have tried to visualize the control scheme:

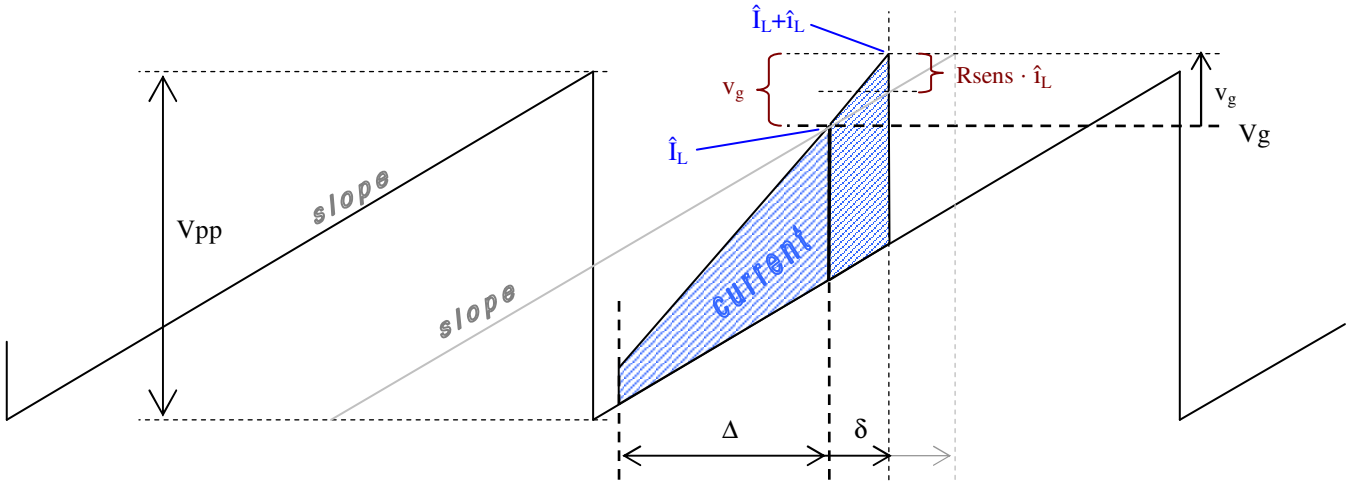



**Figure 17.** CMC modulator gain sketch

In the steady state, the peak current is $\hat{I}_L$, duty cycle is $\Delta$ and the control voltage is $Vg$.
The shown current block is really a voltage block (= Rsens · current) which can be compared to $Vg$ and $Vpp$ in the comparator.
The current block is shown added to the ramp slope, and the sum is compared to the control voltage $Vg$, this is consistent with figure 16.
Now, if a small perturbation $v_g$ is added to the control voltage, the duty cycle will increase with $\delta$ and peak current will increase with $\hat{i}_L$ (did you notice the “hat” symbol for peak value).

By studying the small triangles in the top of figure 17 it is evident (after a little while) that

$$\delta \cdot Vpp + Rsens \cdot \hat{i}_L = v_g \qquad \text{or} \qquad \delta(s) = \frac{v_g(s) - Rsens \cdot \hat{i}_L(s)}{Vpp}$$

This equation is very fundamental for current mode control with any amount of slope compensation, from pure CMC to pure VMC. It is one of all the equations used for deriving the formulae in my loop calculator worksheets.

Figure 17 and the equation are valid for all three basic topologies: boost, buck and buck-boost.

The so-called modulator gain $\frac{\delta(s)}{v_g(s) - Rsens \cdot \hat{i}_L(s)} = \frac{1}{Vpp}$ found here seems to disagree with several authors in the past, many of whom, however, seem to disagree with each others (ref. 3 + 4 …). Not all of them can be correct but there are obviously also more than one correct – or at least usable – model for the pwm modulator.

The probably most significant difference between VMC and CMC is that the CMC open loop is basically only 1st order, whereas VMC is 2nd order. A Current Mode Controlled power stage can be thought of as a controlled current source loaded with a capacitor + a load. My e-book reveals that this is only strictly true in some special cases but anyway it is a fair assumption which gives us good enough results in many practical cases.

The worksheets will also demonstrate that as soon as a ramp is added for slope compensation, a pole re-appears in the controlled current source but usually it is at a high frequency where it does not hurt.

It could be hoped that the unpleasant Right Half Plane Zero in some topologies would also vanish with Current Mode Control. I am sorry to disappoint you. The RHPZ is a fundamental property of the boost, buck-boost and some other converters, and it will stay there, regardless of control method.

## Discontinuous current (DCM)

All three basic converter types can run either with continuous current ($I_L$ always > 0) or with discontinuous current, unless synchronous rectification is always applied. In the latter case, the inductor current can move unbounded over positive as well as negative currents.
Typically, a converter will run through both regions in its operating load range.

In Discontinuous Current Mode the previous discussion and results cannot be used since the equations in DCM are different from those in CCM. For instance, in DCM the 2nd order open loop response seen in the previous section always turns into a first order response, however, for VMC this response can be a very sluggish one. VMC power stages suffer from a huge gain reduction when passing from CCM to DCM. Many of you have seen how miserable the regulation of an output voltage can be when your Voltage Mode Controlled converter operates at low current.

With pure CMC, it appears that the boundary between CCM and DCM does not exhibit this abrupt gain jump. The open loop gain is the same above and just below the DCM boundary. Only when you decrease power well below the boundary, you will see a gradual reduction of open loop gain. This is another great advantage of CMC.

But when you apply slope compensation, the sudden change in loop gain re-appears, however, for normal and moderate amounts of slope compensation, the effect is small.

You can study all these peculiarities by playing with the loop calculators, and the text in my e-book will provide some background explanation.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk







# Boost regulator – elaborated example

Now, let us have a look at an example of what the math worksheets can do for us.
Below, we have a boost converter model with an LC ripple filter in the output. The popular TL431 / LM431, etc. has been used as the error amplifier in this example. There can be one (P1 = 0) or two (P1 = 1-2) feedback points. Two feedback points are often unavoidable when using the TL431. In this example there is also a transconductance amplifier and another operational amplifier in the feedback path. Not all of these gain blocks are normally used at the same time. For example, you can disable the gm block and the following amplifier by setting gm = 1, Cp = Cpp = 0, Rp = 0, Rg = 1, Cg = 1 (1F≈∞) and Cgg = 0.

Pure Voltage Mode Control is when you set Rsens = 0. Pure Current Mode Control is with Vpp = 0. Pure CMC can only be used at duty cycles < 50%. With duty cycle > 50% you must have both $\mathrm{Vpp} > 0$ and Rsens > 0.
Units are implied to be Volt, Ampere, Ω, Farad, Henry, Hz, etc.

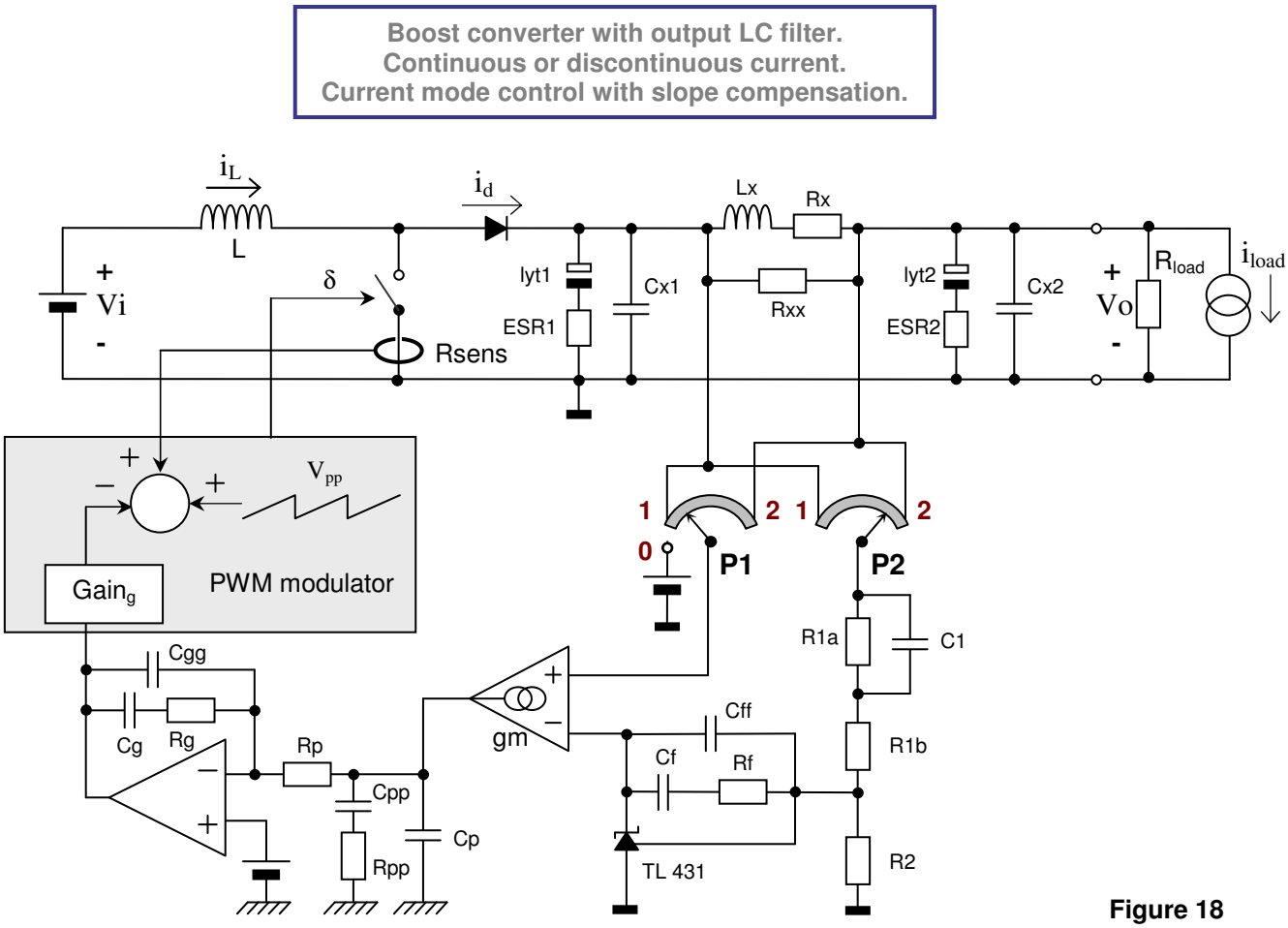



**Figure 18**

The feedback points can be swept continuously between input and output of the ripple LC filter, symbolized by potentiometers. For instance, P2 = 1,5 can be achieved by splitting the damping resistor Rxx in two equal parts and connecting R1a + C1 in the middle. This feature can demonstrate surprising things.

Have a look at the print-out in the next page.
The critical phase is shown as zero in these plots. Whether it is -180 degrees or 0 degrees is a matter of definition and taste.

Output capacitors are small ceramic types with very small ESR. With small capacitors you may really want a ripple filter. But first, let us assume there is no ripple filter: $\mathrm{Lx} = 0$.

Phase margin is 40 – 45 degrees, gain margin is (only!!) 5dB. There is a nice non-ringing step load response.

The effect of the RHPZ is very clear. Here the RHPZ is at 10,6 kHz. In the “open loop gain [dB]” curve it causes the gain to flatten out at > 10kHz while phase goes negative very fast.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Feedback in Switch Mode Power Converters

July 2013

## Load your network variables here :

Inductor : $L \equiv 300 \cdot 10^{-6}$

First output capacitor : $lyt1 \equiv 2 \cdot 10^{-6}$ $ESR1 \equiv 0.005$ $Cx1 \equiv 0$

Filter inductor : $Lx \equiv 0$ $Rx \equiv 0$ $Rxx \equiv 44$

Filter capacitor : $lyt2 \equiv 2 \cdot 10^{-6}$ $ESR2 \equiv 0.005$ $Cx2 \equiv 0$

Load resistance : $Rload \equiv 10000$

Error amp. gain * bandwidth : $f0dB \equiv 2 \cdot 10^{6}$

Error amp. feedback resistor : $Rf \equiv 22 \cdot 10^{3}$

Error amp. feedback capacitor : $Cf \equiv 4.7 \cdot 10^{-9}$

Ripple suppression capacitor : $Cff \equiv 0$

Upper resistor in voltage divider : $R1a \equiv 100 \cdot 10^{3}$

Capacitor in parallel to R1a : $C1 \equiv 0$

Middle resistor in voltage divider : $R1b \equiv 0$

Voltage divider output : $Vref \equiv 2.5$

Transconductance gain [A/V] : $gm \equiv 1$

gm amplifier load resistance : $Rp \equiv 0$

Noise capacitor || Rp : $Cp \equiv 0$

R+C || Rp and Cp : $Rpp \equiv 0$ $Cpp \equiv 0$

Prim. amp. feedback resistor : $Rg \equiv 1$

Prim. amp. feedback capacitor : $Cg \equiv 1$

C || Rg and Cg : $Cgg \equiv 0$

Slope compensation ramp : $Vpp \equiv 0.1$

Current mode constant [V/Apeak] : $Rsens \equiv 0.5$

Fixed modulator gain : $Gain_g \equiv 0.61$

Feedback connection points : $\begin{pmatrix} P1 \\ P2 \end{pmatrix} \equiv \begin{pmatrix} 0 \\ 1 \end{pmatrix}$

**P1 = 1- 2 or 0** **P2 = 1- 2**

Switching frequency : $F \equiv 100 \cdot 10^{3}$

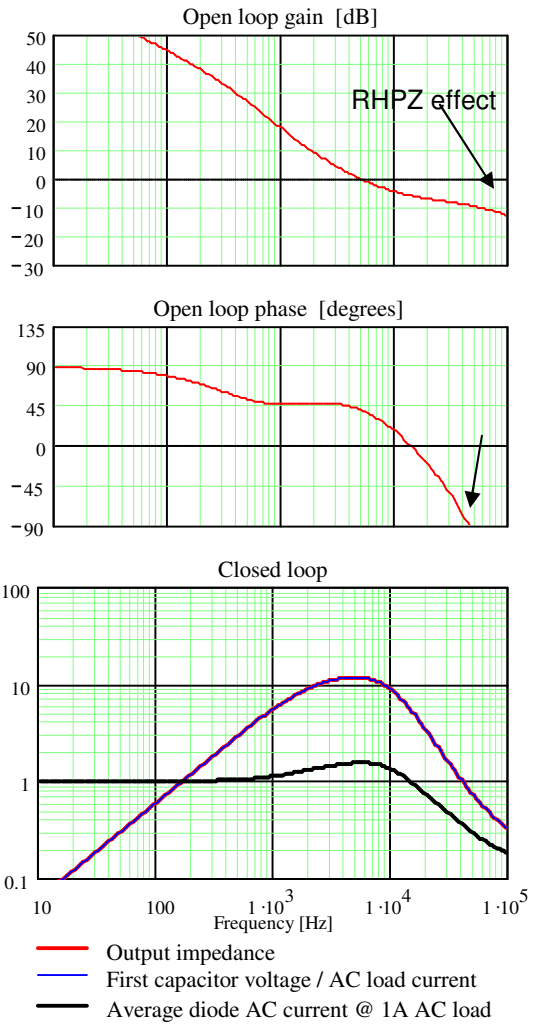
Input voltage : $Vi \equiv 20$

Output voltage : $Vo \equiv 50$

**Power :** $P \equiv 20$ [W]

**Test frequency :** $Fo \equiv 2000$ [Hz]

**Current step :** $Istep \equiv 0.1$ [A]



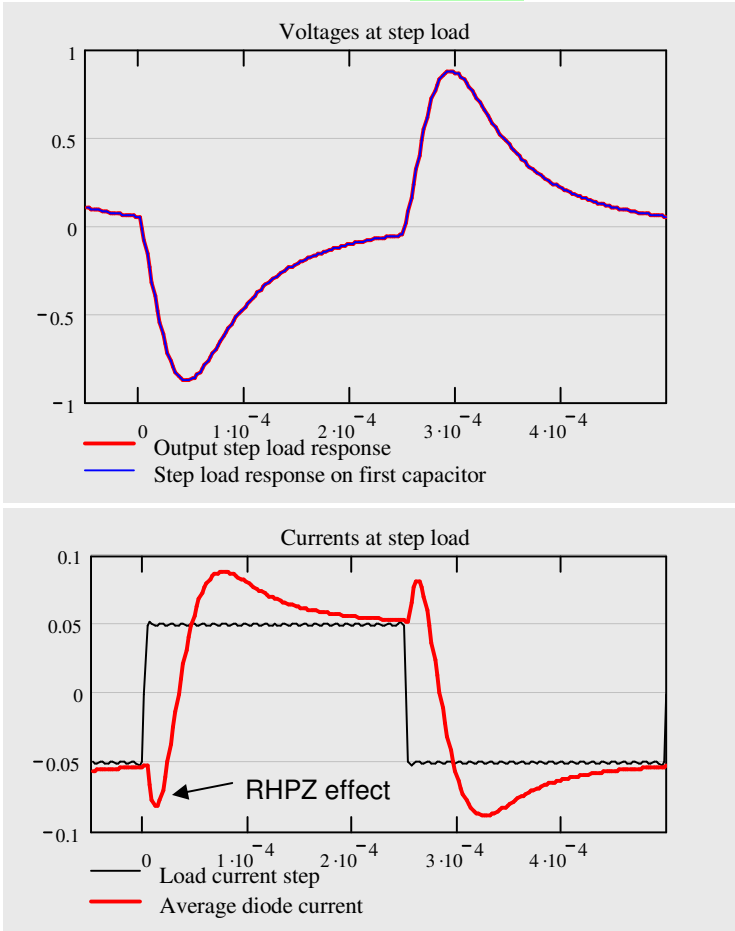




**Figure 19.** no ripple filter

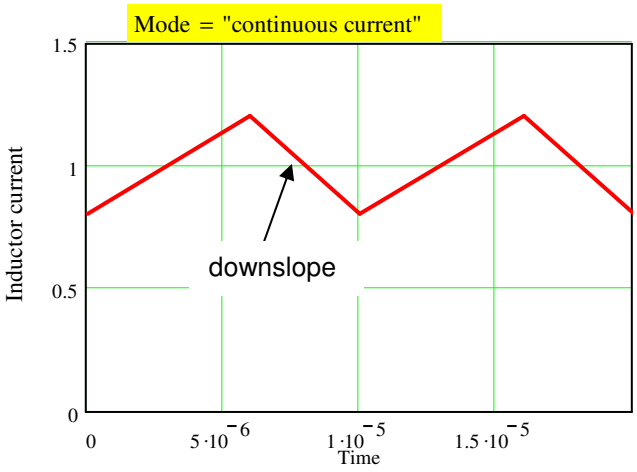
Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Feedback in Switch Mode Power Converters



The inductor current waveform is calculated for each selected working condition. In this case we are in continuous current mode with duty cycle > 50% so slope compensation is needed. The worksheet also calculates the actual and the necessary slope.




Right half plane zero: $\text{rhpZero} = 10.6 \times 10^3$ **[Hz]**

Relative slope: $\frac{\text{slope}}{\text{downslope}} = 0.20$

Minimum slope for stability: $\frac{\text{min\_slope}}{\text{downslope}} = 0.17$

$$\text{slope} = \frac{1}{\text{Rsens}} \cdot \frac{\text{Vpp}}{\text{T}} = \frac{1}{\text{Rsens}} \cdot \text{Vpp} \cdot \text{F}$$

**Figure 20.** Inductor current

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Feedback in Switch Mode Power Converters



Let us try to insert a ripple filter inductor Lx:

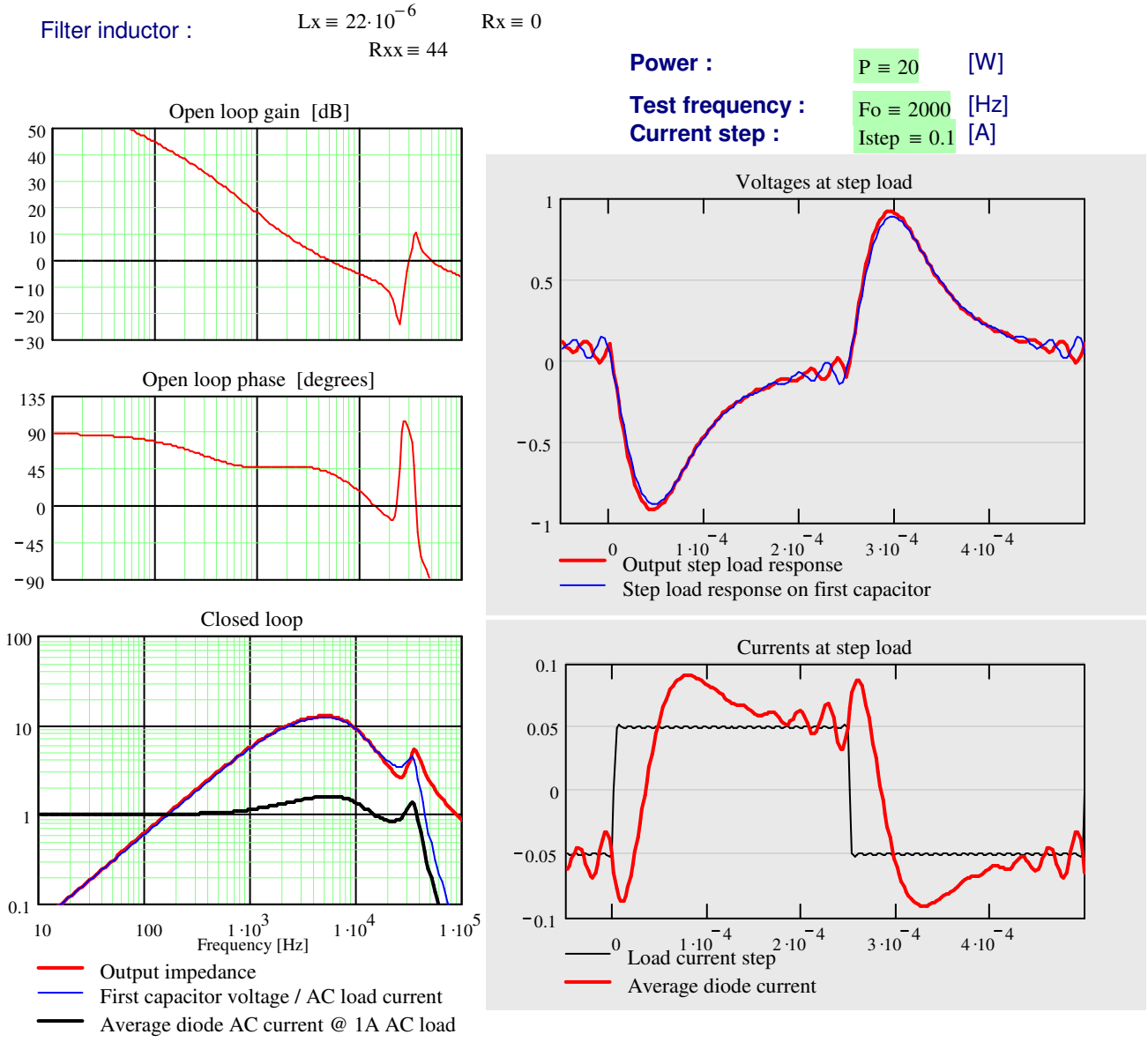



**Figure 21.** Feedback before filter

The feedback point is before the LC filter.
Now the converter is unstable. You see a new peak in the closed loop curves, and oscillations grow up in the time plots. There are three zero dB crossing points. The first still has 40 – 45 degrees phase margin, the second has > 90 degrees but the third crossing has < zero degrees margin. This is where it oscillates.

Do not be fooled by the apparently well damped new resonance peak in the closed loop curves. This peak is sharp only close to the boundary between stability and instability. If the system is deeply unstable, i.e. if the exponentially increasing oscillation grows up very fast, this peak looks small. In extreme cases it can even be difficult to distinguish the peak in the closed loop frequency curves and the growing oscillation can be short and difficult to see. Therefore, be sure to always check the open loop gain and phase, as you would with the results from a network analyzer.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Feedback in Switch Mode Power Converters



Next, we will change the feedback point from before to after the LC filter. One might expect the converter to become even more unstable because the filter adds phase lag above its resonance frequency. But this is not the whole story. As we see, the converter is now stable, although it has a gain margin of only 4 dB which is not advisable. Increasing gm from 1 to 1,6 in this case makes it oscillate at 15 kHz.

The phase delay now continues to increase when passing over the filter's resonance frequency. Self oscillation can only occur at a phase delay of 180 degrees (0 degrees in these plots) which does not occur here when the gain peaks above 0 dB. It is in agreement with Nyquist's criterion for stability in which the point (-1,0) in the complex plane must be encircled by the gain curve in order to become unstable.

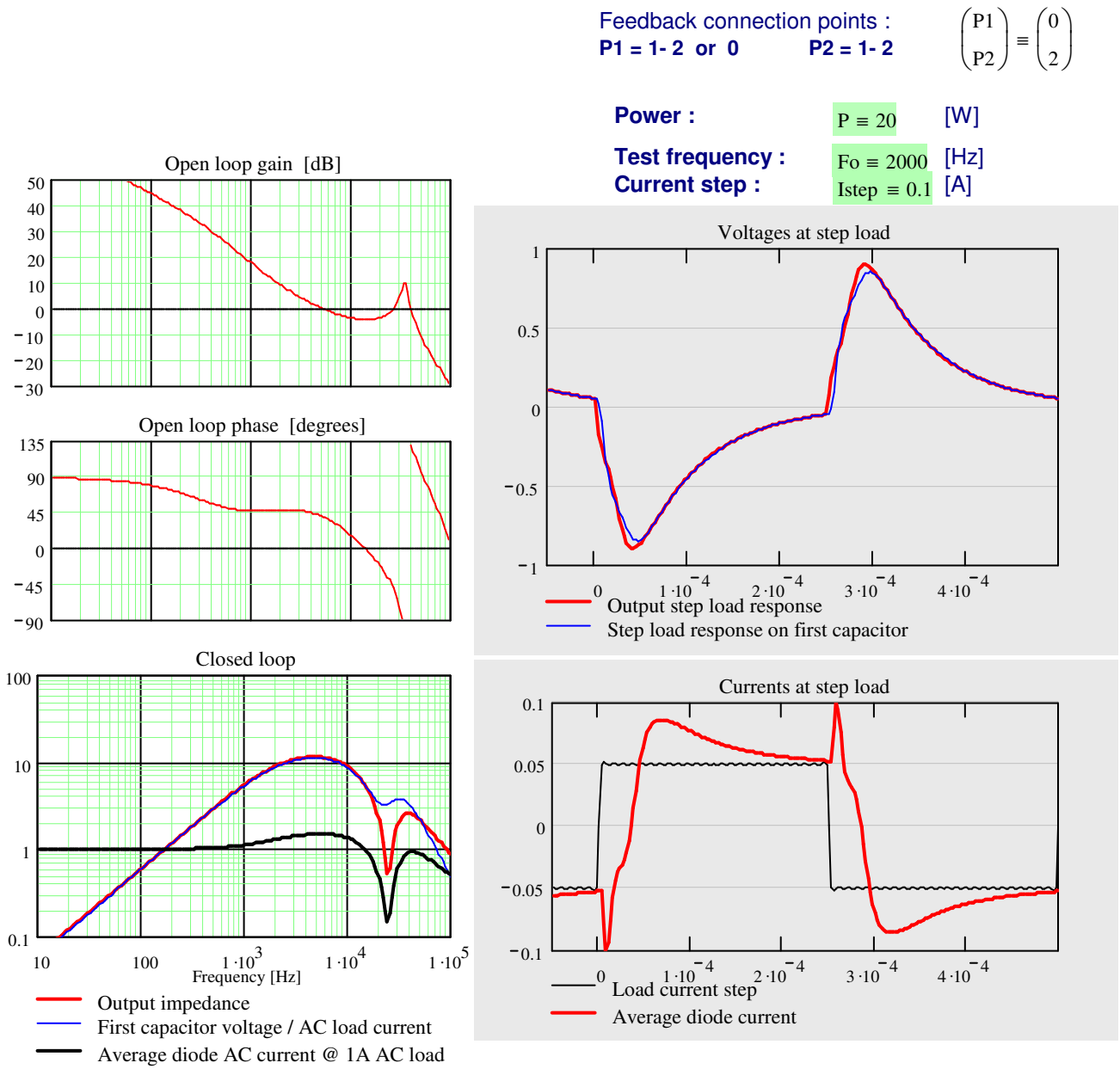



**Figure 22.** Feedback after filter

This result does not imply that you should always connect the feedback point after a filter. Very often – in fact I think in most cases – the best stability is achieved when you connect the feedback point before the filter.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Feedback in Switch Mode Power Converters



Finally we shall see what happens if we slide the feedback point to the middle of the potentiometer with everything else unchanged:

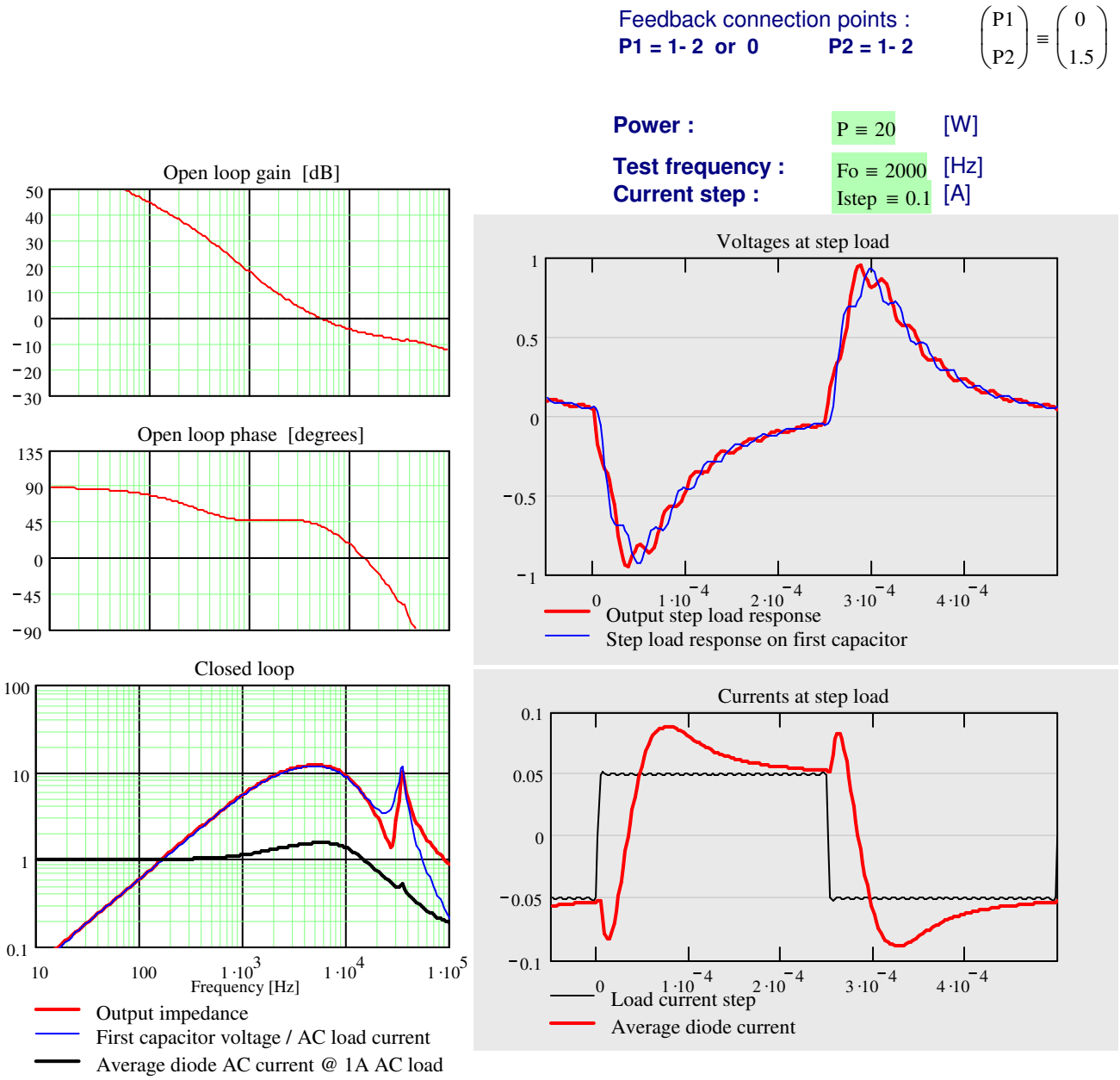



**Figure 23.** Feedback in middle of filter

This is another funny thing. Now the open loop gain and phase are the same as without a ripple filter inductor. The filter resonance is not visible to the loop and the “average diode current” looks like with no filter inductor, although the output voltages before and after the filter ring vividly.

There is a down-to-earth explanation for this phenomenon. Can you figure out what it is? (Hint: look at the voltage waveforms).

## Other topologies and applications

As mentioned, the methods of the three basic Pulse Width Modulated converters Buck, Boost, and Buck-boost can be used also in most of their derived topologies. Buck-derived are for instance the forward, the push-pull forward, the full bridge forward. The flyback converter is one of the most used buck-boost derived topologies. Others are the Sepic, the Cuk and the Zeta converters, however they share only the steady-state equations with the buck-boost, not the dynamic equations. Concerning regulation and feedback, Sepic, Cuk, and Zeta converters are more complicated than the buck-boost, containing more poles and Right Half Plane Zeroes etc.

Another class of converters are the resonance converters, of which the LLC converter has become particularly popular. Resonance converters are strongly non-linear in their regulation characteristics, and some studies of LLC in the past have revealed poles and zeroes in their dynamics which appear, disappear and move around in an apparently chaotic way when sweeping through the operating range of load and transfer ratio (ref. 8). Optimizing the regulation of such converters is virtually impossible, and I have seen more than one LLC which was self oscillating at some working point. This is one severe drawback of resonance converters. Apart from that, resonance converters can be extremely efficient converters with low noise. The problem can be solved by controlling them with Charge Mode Control – an alternative control method which can transform the resonance power stage into a controlled current source, like that of a Current Mode Controlled buck stage. Charge Mode Control was discovered by me in 2003 and patented by my customer Bang & Olufsen (ref. 6).

Most often, a power supply must provide a constant output voltage, but some times you want to keep a controlled and either constant or variable output current, for instance in a battery charger or an LED driver. In such cases you must use a feedback model where current, not voltage, is the input for the error amplifier. Such converters will also need to incorporate a maximum allowed output voltage. In some load conditions this maximum voltage will be reached, in which case the current feedback must turn into a voltage feedback. This means you must consider two feedback loops which should both be stable.

Whether you have a controlled output voltage or current, you may also find applications where you want to control the output quantity with a variable reference, either a slowly or a fast varying reference signal. In other words, to use the power supply as a kind of power amplifier. Then you need a tool to see how well and how fast your power supply will follow a moving reference signal. Large output capacitors will cause a poor or slow performance, so you must use small output capacitors, which always makes feedback design more critical and difficult.

Using an SMPS as a power amplifier requires a different approach, concerning the calculation tool. My e-book also explains how to write the calculator for an SMPS power amplifier to show the response to a step reference signal. It is in fact less complicated than to calculate the output impedance. I have made some worksheets with this feature but at present not for all topologies.

As we can see, there are big diversities in what you may need to calculate. Therefore you will find a lot of applications in which the commonly used models and tools do not provide the solution for you. This is another reason why you should be able to create your own application specific tools.
I hope my mathcad worksheets and my e-book will encourage many of you to do just that.

As a third means of presenting my tools, I am planning to write a PowerPoint show, demonstrating a lot of practical results, educational examples, peculiarities, unexpected behaviour etc. One maybe unexpected recognition is written in a chapter in the e-book and re-written in the next two pages.

The presentation could be made at seminars, either open seminars for everybody or at local seminars at companies with interest in practical feedback. I am open to ideas about that.

It is my hope that my mathcad feedback tools will inspire you to dig deeper into the understanding of feedback issues than you would otherwise have done. My tools are quite different from what you encounter from other sources, for instance on-line tools from IC manufacturers or other design or analysis tools for purchase or licensing.

There are so many ways to attack technical challenges like feedback design in switch mode converters, some are more accurate than others, some are faster and easier to use than others.
I hope you will find my tools to be one of the more attractive contributions to the engineering world.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



# Sampling delay?

I would like to show another aha-experience done while writing my e-book. An experience which also highlights the limitations of the human mind.

We know from regulation theory that signal delays in a feedback loop are equivalent to additional phase lag which can cause trouble and instability. So if there are any delays in the power stage, we need to know about it.

Are there any delays in a buck power stage? Basically no – an answer which can be hard to understand. Try to follow the following reasoning for Voltage Mode Control:

The inductor current $I_L$ is a triangle with up-slopes and down-slopes at the switching frequency. The inductor current appears as the integral of the voltage over the inductor, and the low frequency content of the inductor current appears by integrating the average inductor voltage pr. cycle.
So is there any delay from the control signal to the inductor current when using duty cycle control?
Or more correctly: is there any delay from control signal to duty cycle, and thus to average inductor voltage?

Thinking of the way the duty cycle can be generated: by comparing a sawtooth to a control "DC" signal (which is usually derived from a feedback signal) we can convince ourselves that there must in average be a delay from the control signal to the inductor voltage, and thus a delay from control signal to inductor current which we have not yet accounted for.
Suppose the control signal takes a small jump, it will not be immediately visible on the duty cycle. We have to wait for the next crossing between the ramp and the control signal, before the duty cycle can be adjusted, which can be from zero to one switching cycle T later. In average we should expect a delay from control signal to duty cycle of ½·T, and thus an extra delay in inductor current of ½·T, which is not completely negligible.
Do you agree?

Let us try to look at this in an illustration:

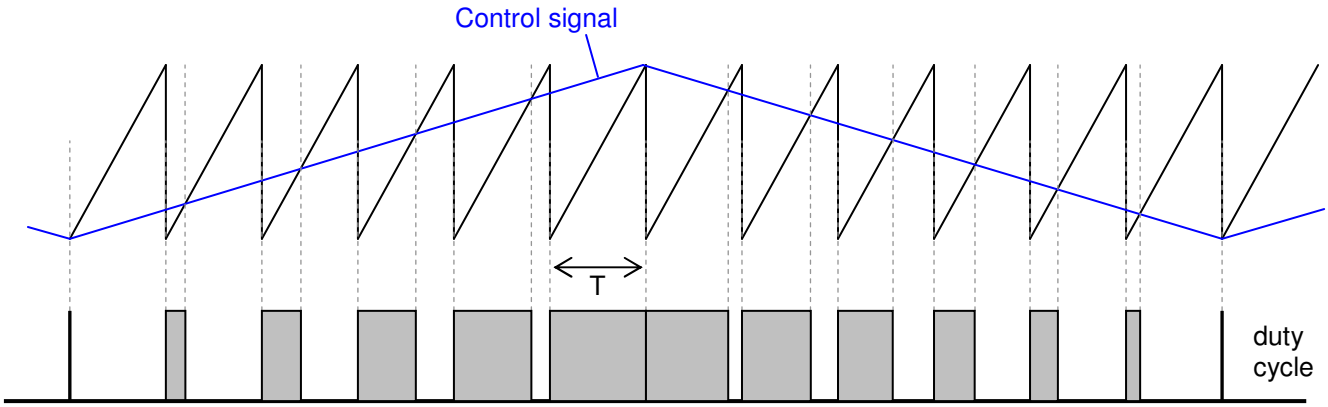



**Figure 24**

Here a "slowly" varying triangle control signal is compared to a ramp with period T.
The output is a logic signal indicating the instantaneous duty cycle.
What we are looking for is a delay in duty cycle in relation to the control signal. This is not really easy because duty cycle is not a continuously smooth function like the control signal. However when looking for a "gravity centre" in the duty cycle this centre should be displaced ½·T to the right of the top of the control triangle.

But it is not !
The gravity centre coincides exactly with the control signal top.
The expected delay is not there. So the "average" content of the inductor voltage will not be delayed compared to the control signal. The previous arguments leading to a delay must be based on a misconception of facts.

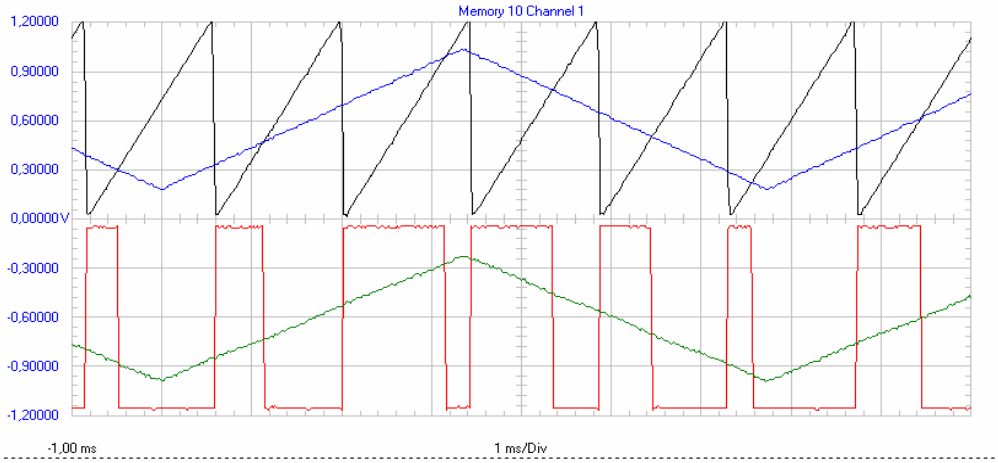
Once I attended an SMPS seminar where the lecturer claimed that there is no such "sampling delay" in a buck converter, I didn't believe him. But that was a lot of years ago.

To prove the absence of the sampling delay I have made the above experiment in real life. Injected a fast ramp and a slow triangle to the inputs of an analogue comparator and studied the pulses on the comparator output with an oscilloscope.
To get a more precise picture of the "gravity centre" of the output pulses I let the scope calculate an averaged plot of a lot of sweeps in which the ramp position is random compared to the triangle.
As you see below, the averaged duty cycle signal is an exact copy of the control signal.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk



This is in fact very fortunate since the expected delay would have reduced the possible performance of buck feedback loops considerably.




PWM modulator.
Upper traces: ramp signal and modulator triangle.
Ramp and modulator triangle are fed to comparator inputs.
Lower traces: PWM output from comparator and averaged PWM.

**Figure 25**

On the other hand, in CMC there is a delay. Not a large one but if you want to squeeze your feedback loop to the utmost performance you should not neglect it. This delay is included in my worksheets and described in the belonging e-book.

The boost and the buck-boost power stages also contain an additional delay which are described in the e-book and implemented in the worksheets. How to correctly understand and model these delays is also an area of some dispute among the feedback gurus, however, for practical design one model can be as good as another one.

Runo Nielsen
Kildebjerggaard 3
5690 Tommerup, Denmark
telephone : +45 64 76 10 02
email :runo.nielsen@tdcadsl.dk
www.runonielsen.dk







# References (updated September 2018)

1 Unitrode application note U97: Modelling, Analysis and Compensation of the Current-Mode Converter.
http://focus.ti.com/lit/an/slua101/slua101.pdf

2 Venable Industries: Current Mode Control
https://venable.biz/uploads/files/05-Technical-Paper-Current-Mode-Control.pdf

3 Ray Ridley's PHD dissertation: A New Continuous-Time Model for Current-Mode Control. 1990,
chapter 2 and 3.
Download it from http://www.ridleyengineering.com/images/current_mode_book/CurrentModeControl.pdf

4 Rendon Holloway et al: Model Current-Mode Control With Ease and Accuracy. 2008.
https://iie.fing.edu.uy/publicaciones/2008/HE08/HE08.pdf

5 Ray Ridley: Analyzing the Sepic Converter. 2006
http://cdn14.21dianyuan.com/download.php?id=59460

6 Bang & Olufsen patent: WO 2005/046037 – 2005-05-19
Title: "Charge Mode Control of a Serial Resonance Converter"
Inventors: NIELSEN RUNO (DK); CHRISTENSEN SOEREN KJAERULFF (DK).
http://v3.espacenet.com/textdoc?DB=EPODOC&IDX=WO2005046037&F=0

7 Texas Instruments: The right half plane zero – a simplified explanation.
https://edoc.site/the-right-half-plane-zero-pdf-free.html

8 ST : AN2644 - An introduction to LLC resonant half-bridge converter. 2008
http://www.st.com/st-web-ui/static/active/en/resource/technical/document/application_note/CD00143244.pdf?s_searchtype=keyword

9 Ray Ridley: RidleyWorks. SMPS design software replacing the older Power 4-5-6.
Rent it or download an appetizer at
http://www.ridleyengineering.com/design-center-ridley-engineering.html

10 Dennis Feucht: Current-Loop control in Switching Converters. Part 1 to 7. 2011- 2012.
Part 1: http://www.how2power.com/newsletters/1109/articles/H2PowerToday1109_design_Innovatia.pdf
Part 2-7: find them at http://www.how2power.com/index.php.

11 Ray Ridley: A More Accurate Current-Mode Control Model.
https://www.ti.com/seclit/ml/slup122/slup122.pdf

12 Runo Nielsen: Half bridge converter, DC balance with current signal injection. 2012.
http://www.runonielsen.dk/Half_bridge_control.pdf

13 Vatché Vorpérian: Simplified Analysis of PWM Converters Using Model of PWM Switch,
Part I: Continuous Conduction
Part II: Discontinuous Conduction Mode
IEEE Trans. Aerosp. Electron. Syst., vol. 26, no. 3, pp. 49M96, 1990.