
Understanding the Feedback Loop in a Buck Converter

Runo Nielsen

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Abbreviations and symbol list

SMPS	Switch Mode Power Supply
PWM	Pulse Width Modulator
CMC	(peak) Current Mode Control
VMC, DCC	Voltage Mode Control = Duty Cycle Control
CCM	Continuous Current Mode: Inductor current is always > 0 .
DCM	Discontinuous Current Mode: Inductor current = 0 in fractions of the switching period.
ESR	Equivalent Series Resistance
DC	'Direct Current'. Current, voltage, or other signal with a constant positive or negative value
AC	'Alternating Current'. Current voltage, or other signal with a variable value and average = 0

List of symbols

V_i	Fixed input voltage of the buck power stage
$V_o + v_o$	Buck output voltage, steady state + perturbation
$V_s + v_s$	Average voltage pr. cycle after the switch, steady stage + perturbation
$V_g + v_g$	Control voltage, steady state + perturbation
V_{pp}	Slope compensation ramp or duty cycle control ramp, Volt peak-peak
$V_{sens} + v_{sens}$	Current sense voltage during the on-time, steady state + perturbation. $V_{sens} = I_L \cdot R_{sens}$
$I_L + i_L$	Inductor current, steady state + perturbation
$\hat{I}_L + \hat{i}_L$	Inductor peak current, steady state + perturbation
$I_{pp} + i_{pp}$	Inductor ripple current, steady state + perturbation. $\hat{I}_L + \hat{i}_L = I_L + i_L + \frac{1}{2} \cdot (I_{pp} + i_{pp})$
$I_o + i_o$	Output current into the load resistor R_{load} , steady state + perturbation
F	Switching frequency
T	Switching period. $T = 1/F$
t	Continuous time variable
$s = \sigma + j \omega$	Complex frequency for Laplace transform. ω is radial frequency
$\Delta + \delta$	Duty cycle, steady state + perturbation
L	Inductance of buck inductor
C_o	Output capacitor
ESR	Equivalent series resistance of output capacitor
R_{sens}	Current sensor, sensing current in the on-time. Unit = V/A
R_{sens}	Current sensor multiplied to a correction factor describing subharmonic behaviour
R_L	Copper resistance in the buck inductor
R_{load}	Dynamic load resistance. Does not have to be V_o/I_o . It can be infinite, or even negative
Z_{load}	Impedance of output capacitor + R_{load}
Z_L	Impedance of inductor
Powergain	Gain from control input v_g to output current i_L [A/V]
Vpowergain	Gain from control input v_g to output voltage v_o [dB]
upslope	Sensed slope of inductor current in the on-time
downslope	Sensed slope of inductor current in the off-time, defined as a positive number
slope	Slope of compensating ramp. Slope = V_{pp}/T
pro, pro _o	Error progression factor from one switching cycle to the next. pro _o is with $V_{pp} = 0$
HFcor(s)	Multiplying this correction factor to R_{sens} is all it takes to describe subharmonic behaviour
ω_o	Radial resonance frequency of the analog model. Also used with a corrected value at $\pi \cdot F$
Q, Q_o	Q factor of an analog ringing resembling that of subharmonic error decay. Q_o is with $V_{pp} = 0$
d	Damping factor of the $(L + C_o)$ resonance in the buck transfer function in VMC

Abstract

Small signal feedback loop analysis of pulse width modulated (PWM) converters have been treated by many authors during time.

In this article I try to show an alternative way, using math that most electronic engineers can master. It leads to simple and ready-to-use equations for the transfer function of the buck power cell in Continuous Current Mode.

It covers both Voltage Mode and Current Mode Control.

Part of the derivation is to find the basic equation for the PWM modulator. It is derived from simple geometric observations, however this modulator gain seems to be the subject of heavy disagreement among SMPS experts.

Subsequently, a new and surprisingly simple equation is found to describe the well-known subharmonic behaviour of a current mode controlled PWM power cell in Continuous Current Mode:

$$HF_{cor}(s) = s \cdot T \cdot \left(\frac{1}{1 - e^{-s \cdot T}} - \Delta \right)$$

This strange (complex) correction factor is simply multiplied to the (real) current sensor gain R_{sens} in the above mentioned PWM modulator equation. By doing so, the apparent "resonance peak" at half the switching frequency, when using peak current mode control, is included in the power cell's transfer function.

The correction factor does not involve component values or control data, only operating duty cycle and switching frequency. (!!)

I admit, the HF_{cor} equation defies my imagination deeply, but plotting the result in a calculator reveals its power.

Multiplying this correction factor to R_{sens} applies to buck as well as boost and buck-boost.

Gain and phase of the power cell's transfer function can be plotted with any suitable math software.

The modulator gain expression and the subharmonic correction factor have been verified for buck and buck-boost by simulations in Simplis, and the controversial modulator gain expression has further been confirmed by experimental results in a specially built buck power stage. The documentation of the verification is not part of this article.

1 Introduction

The present article was written after many years of designing Switch Mode Power Supplies for the industry.

Switch mode power supplies comprise an ever increasing wealth of topologies, all of them containing inductors and/or transformers, capacitors, and fast semiconductor switches like mosfets and diodes. An on-going endeavour is to come closer and closer to the magic efficiency of 100%.

However, topologies and efficiency will not be the topic of this article. This article will concentrate on one well-known topology: the buck (step down) converter and how to understand its regulation mechanism. Many papers during time have dealt with that topic, so why do I want to go into it once again?

The fact is that most electronic engineers are unable to follow the techniques and advanced mathematic abstraction used in those papers. I am one of those engineers.

Therefore "I did it my way", although I am not a big fan of the singer of that song. I believe I found a way through the math that is relatively easy to follow for an engineer, leading to equations directly usable in any math software.

Various software is available that will help you design power supplies and their regulation loops. Some is for purchase or licensing, some is available for free on SMPS IC-manufacturers' websites. The software can be fine to help us with good and fast SMPS designs, but none of them provide a deep understanding of the physics and modelling that lie behind. A drawback of this kind of software is that it does not always tell us under which conditions it is valid or inaccurate. Another drawback is that it is not very flexible regarding variation of circuit details or control IC. You are forced to work with the options given by the software.

The object of this article is to de-mystify the theory behind feedback loop design in SMPS. I want to enable you as a design engineer to look behind the curtain and I want to encourage you to build your own calculators for your dedicated purposes. Or buy one of mine and modify it to fit with your needs. SMPS feedback loop design is difficult but should not be inaccessible magic.

An SMPS usually contains a feedback loop to regulate and maintain output voltage, output current or some other parameter. Many SMPS designers are familiar with the notorious struggle with feedback loops and stability. My struggle has, during the years, led to an assortment of loop calculation tools built in Mathcad to help me in my design of stable and fast responding power supplies.

It's a long time since I have designed a self oscillating SMPS prototype, as it frequently happened in the first part of my career.

During time these tools have evolved from relatively simple and with limited applicability to advanced tools covering many SMPS topologies and their most popular operating and control modes. You can read more in ref. 11.

For Pulse Width Modulated (PWM) types of converters the latest improvement of my tools was the inclusion of the subharmonic phenomenon observed with CMC. It has long been known that if we exceed 50% duty cycle with CMC (in CCM), the power cell becomes unstable and starts to oscillate at half the switching frequency ($F/2$), even before the outer feedback loop is closed. Below 50% the power cell does not oscillate but still can respond to a control step with a behaviour resembling a damped ringing at $F/2$. This is what we call subharmonic behaviour. Even though the power cell is not self oscillating below 50%, it may cause an outer feedback loop to become unstable at $F/2$.

In particular I want to share with you a way that I recently found to describe this phenomenon mathematically. A quite long explanation leads to one surprisingly simple and accurate equation, which is different from that found in other literature (ref 3 and 8).

I will try to lead you gently into the techniques that I found useful in the modelling of the power stage of a PWM controlled SMPS, exemplified by the buck converter - the most straightforward one of the three basic PWM controlled topologies.

I believe my approach is more or less similar to the State Space Averaging technique used by Dr. Slobodan Cuk and late Dr. Middlebrook in the 1970's, however my approach does not use matrix algebra, only standard high school math. I am not skilled enough to handle matrix algebra, as I believe is the case for many of my readers too. But don't be mistaken. It is amazing what you can do with basic high school math.

Using matrix math is not paramount for state space averaging, although I believe it does yield simple looking closed form solutions, suitable for computer calculus. What is really important in the concept of state space

averaging is that it deals with **average values of currents and voltages during each switching cycle**. Using state space averaging, all information on switching phenomena and switching ripple is neglected. This can be justified for the feedback loop which by nature deals with “low” frequencies. Output signals are assumed to be DC, on which deviations are of low frequency nature compared to the switching frequency. Switching frequency ripple must be filtered out in the loop to fulfil the basic ideas of feedback and regulation.

The total feedback loop in an SMPS system consists of several elements, most of which can be described by the classical methods involving s-plane theory (Laplace transform). Most electronic designers are familiar with these methods. Such circuit elements are for instance resistive and capacitive voltage dividers, linear amplifiers with local RC-feedback, opto couplers (many consider an opto coupler a frequency independent device – this is most often not the case), LC filter stages etc. The total open loop gain and phase is usually calculated by adding the dB's and the phase angles of each individual stage.

However there is one big issue, which is not covered by basic knowledge of electronic engineers: How to describe and calculate the gain and phase of the power stage.

I am going to show you the simple derivation of the control equations for a buck power stage in CCM, first in DCC, then in the general case covering DCC as well as CMC and any combination in between. And I am going to reveal how the subharmonic behaviour can be modelled and included in a surprisingly simple, yet accurate way.

As an appetizer to motivate you to continue reading, it could be a good idea to start with ref. 11.

I am aware that some of my statements and methods can be controversial among SMPS gurus. I will discuss this in more detail in appendix 1. However, I believe there can be more than one good model of an SMPS power stage. As long as the methods we use to describe a chosen model are consistent and well-founded, the outcome should be a good description of reality.

Models should always be verified with examples from real circuits or simulations. Simulations can be preferred over real circuits because you can make ideal models of inductors, resistors, capacitors, and switches without parasitic effects. I also know that not everyone will agree on that statement.

Simplis is a simulation software which is especially good for this purpose. A pity that so many don't know Simplis (ref. 13). I didn't until recently.

2 Basic buck control

2.1 Basic buck properties

The fixed-frequency buck (step-down) converter is the topology that is most usually studied in literature. For instance many manufacturers of DC-DC converter ICs publish application notes dealing with the design and compensation of the buck converter with voltage mode or current mode control. Such application notes tend to be a bit superficial, however probably good enough for each individual application. Some manufacturers also make software available which can help the designer to obtain stable feedback loops, e.g. by showing open loop phase and gain curves, and some times also a step load response can be calculated by the software. But such software seldom gives you much feeling or understanding of the theoretical background in your buck converter design.

With this article I want to give you a good feeling of the properties of the buck power stage with different kinds of control.

Figure 2.1.1 and 2.1.2 show the basic buck converter and its voltage waveform. A copper resistance R_L is included in the inductor.

Here we will study the dynamic properties of the buck converter in CCM only. Its properties in DCM can be much different.

As is common practice, steady state values are described by **UPPER CASE** letters, while **lower case** letters are used for perturbed values, i.e. small signal deviations from steady state.

All currents and voltages can be described as a sum of a steady state value (DC) and a small signal, time dependent or frequency dependant deviation (AC). What's interesting in feedback loop analysis is the small signal - or dynamic - part.

Switches and diodes are considered ideal, i.e. no on-state voltage and no off-state current.

The steady state transfer function for the buck is linear as shown in (2.1.1), in contrary to the boost and buck-boost converters (ref. 11). Linearity is a very desirable property.

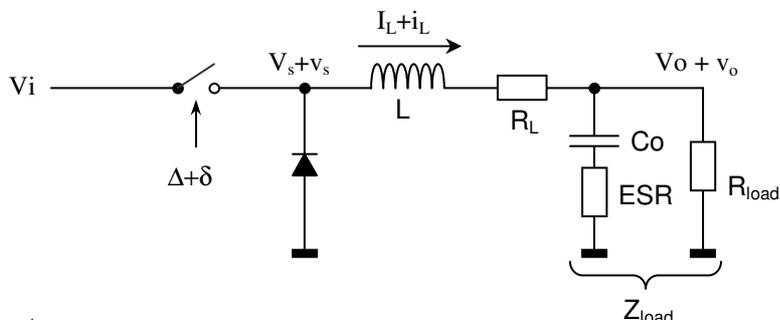


Figure 2.1.1

Steady state buck equations in CCM (neglecting diode voltage drop):

$$V_s = \Delta \cdot V_i \quad (2.1.1)$$

$$V_o = \Delta \cdot V_i - I_L \cdot R_L \quad (2.1.2)$$

$$\Delta = \text{approx} \frac{V_o}{V_i} \quad (2.1.3)$$

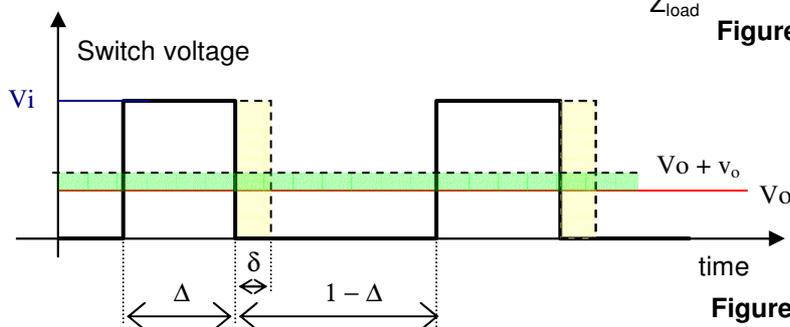


Figure 2.1.2

(2.1.1) states that the average switch voltage in one cycle is input voltage multiplied by duty cycle. Since the average voltage over an inductor is zero, $V_o = V_s$ minus voltage drop over the resistor (2.1.2). Neglecting R_L , duty cycle is $\Delta = V_o/V_i$ (2.1.3) - a well known property for the buck converter.

Like steady state properties, dynamic properties are studied by considering average values of voltages and currents pr. switching cycle.

For the dynamic properties we must consider small perturbations around a selected DC working point.: δ around Δ for duty cycle and v_o around V_o for output voltage. Input voltage V_i is assumed to be constant.

We can write the following expressions (2.1.4) to (2.1.7).

(2.1.4) follows from (2.1.1) because (2.1.1) is linear:
$$v_s = \delta \cdot \frac{dV_s}{d\Delta} = \delta \cdot \frac{V_s}{\Delta} = \delta \cdot V_i$$

(2.1.5) is the Laplace transform of (2.1.4).

(2.1.6) is simply the law of inductors: $V = L \cdot di/dt$ applied to the small signal part of inductor current.

(2.1.7) is the Laplace transform of (2.1.6) with v_s from (2.1.5) inserted and then solved for $i_L(s)$. Differentiation in time domain becomes multiplication with s in Laplace domain.

$$v_s = \delta \cdot V_i \quad (2.1.4)$$

$$v_s(s) = \delta(s) \cdot V_i \quad (2.1.5)$$

$$\frac{d}{dt} i_L = \frac{1}{L} \cdot (v_s - v_o - R_L \cdot i_L) \quad (2.1.6)$$

$$i_L(s) = \frac{\delta(s) \cdot V_i - v_o(s) - R_L \cdot i_L(s)}{s \cdot L}$$

$$i_L(s) = \frac{\delta(s) \cdot V_i - v_o(s)}{s \cdot L + R_L} \quad (2.1.7)$$

In (2.1.7) we can eliminate $v_o(s)$:

$$i_L(s) = \frac{\delta(s) \cdot V_i - i_L(s) \cdot Z_{load}(s)}{s \cdot L + R_L}$$

and solve for $i_L(s)$:

$$\frac{i_L(s)}{\delta(s)} = \frac{V_i}{s \cdot L + R_L + Z_{load}(s)} \quad (2.1.8)$$

We can also write:

$$\frac{v_o(s)}{\delta(s)} = \frac{i_L(s)}{\delta(s)} \cdot Z_{load}(s) = \frac{V_i}{\frac{s \cdot L + R_L}{Z_{load}(s)} + 1} \quad (2.1.9)$$

(2.1.8) and (2.1.9) are the small signal transfer functions from duty cycle to output current and output voltage respectively. As long as we use pure duty cycle control, these equations are enough to describe the power stage transfer function in continuous current mode.

Usually the output consists of a large capacitor, typically an electrolytic capacitor C_o with some equivalent series resistance ESR.

If we insert $Z_{load}(s) = \frac{1}{s \cdot C_o} + ESR$

(2.1.9) turns into

$$\frac{v_o(s)}{\delta(s)} = V_i \frac{ESR}{L} \cdot \frac{s + \frac{1}{ESR \cdot C_o}}{s^2 + \frac{R_L + ESR}{L} \cdot s + \frac{1}{L \cdot C_o}} \quad (2.1.10)$$

This is a 2nd order transfer function with one real negative zero and two (normally) complex poles.

If (2.1.10) is compared to the normalized form $\frac{v_o(s)}{\delta(s)} = V_i \frac{ESR}{L} \cdot \frac{s + \text{zero}}{s^2 + s \cdot d \cdot \omega_o + \omega_o^2}$ (2.1.11)

we see a resonance frequency and a damping factor d: $f_o = \frac{\omega_o}{2 \cdot \pi}$ $f_o = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_o}}$ $d = \frac{R_L + ESR}{\sqrt{\frac{L}{C_o}}}$ (2.1.12)

In this derivation we have not taken the load resistor R_{load} into account. A load resistor will increase the damping factor, i.e. flatten out the LC resonance peak which is good. But stability should not rely on a load resistor. If the load happens to be a pure current source the equivalent load resistor is infinite. And if you load the output with another SMPS, the dynamic load resistor can even be negative.

The final formulae (2.1.8) and (2.1.9) will take any dynamic load resistance – positive or negative – into account.

The buck transfer function could have been written down by simple inspection of the circuit which can be considered an LC low pass filter with the input signal $\delta \cdot V_i$. This would immediately lead to (2.1.9).

The resonance frequency and damping factor (2.1.12) are constant versus input and output voltage and load – an attractive property which the boost and buck-boost converters do not have. So the buck converter is linear as well as invariant to load and step-down ratio, provided of course that we stay in CCM.

2.2 Buck with Current Mode Control

In the previous section the buck converter was analyzed in the so-called Voltage Mode Control or as I prefer to name it: Duty Cycle Control (DCC). This is the control scheme known for the longest time. In DCC the control circuit has no information about inductor current so something extra must be done to protect against overload situations.

Peak Current Mode Control (CMC) is another control method which has been increasingly popular since the 1970's. Many IC manufacturers even prefer CMC over DCC because CMC can turn the complex double pole in (2.1.10) into a real single pole, thus facilitating feedback loop design, and because CMC has inherent current limiting and overload protection. See more in ref. 11.

In CMC the switch is still turned on by a clock generator. Inductor current I_L is sensed in the on-time of the switch according to figure 2.2.1 and the switch is turned off again when the inductor current reaches a predefined value which depends on a control voltage V_g .

If the duty cycle can be $> 50\%$ (if $V_o > 0,5 \cdot V_i$) we need slope compensation to avoid subharmonic oscillation (ref. 1 and many others). Slope compensation is introduced by adding a positive ramp V_{pp} to the sensed current V_{sens} . Or by adding a negative ramp to V_g . Much more about that later.

The model in figure 2.2.1 can be used for buck converters with slope compensation – in fact it can describe both pure CMC, pure DCC and all combinations in between. For pure CMC $V_{pp} = 0$. For pure DCC $R_{sens} = 0$. Using slope compensation in CMC is equivalent to introducing a bit of DCC again, which we must do at duty cycles $> 50\%$. Therefore we need the general model like the one in figure 2.2.1.

We must now try to find the power transfer function from control signal v_g to inductor current i_L (which is = output current in a buck).

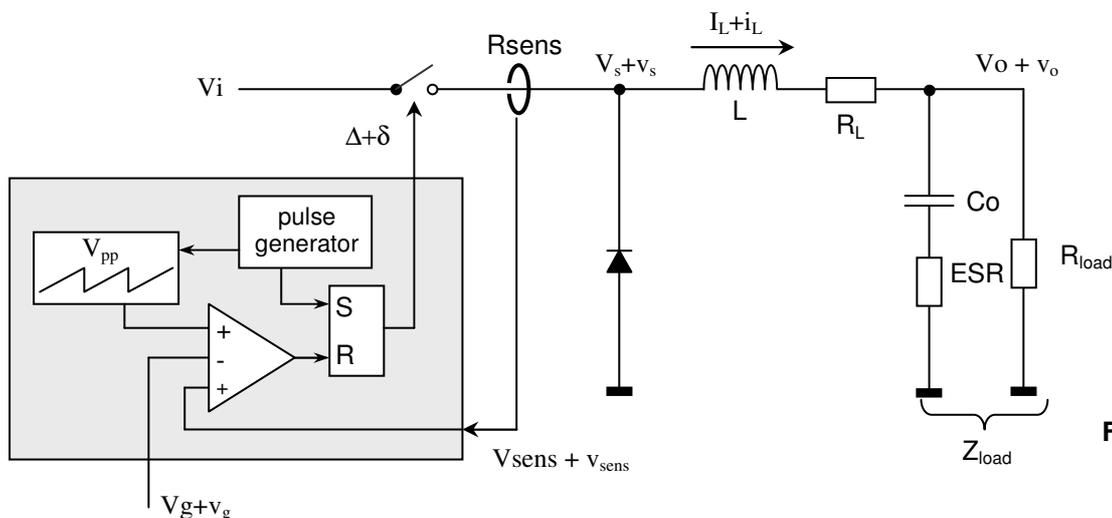


Figure 2.2.1

In figure 2.2.1, obviously the duty cycle depends on $V_g + v_g$ as well as $V_{sens} + v_{sens}$, since both are inputs to the comparator which determines $\Delta + \delta$. In other words, δ is a function of both the control variable v_g and the peak current \hat{i}_L . (note the "hat" symbol for peak value).

Let us first have a look at figure 2.2.2. Here I have tried to visualize the control scheme.

In the steady state, the peak current is \hat{I}_L , duty cycle is Δ and the control voltage is V_g .

The current block R_{sens} · current is compared to V_g and V_{pp} in the comparator.

The current block is shown added to the ramp slope, and the sum is compared to the control voltage V_g , this is consistent with figure 2.2.1.

Now, if a small perturbation v_g is added to the control voltage, the duty cycle will increase with δ and peak current will increase with \hat{i}_L .

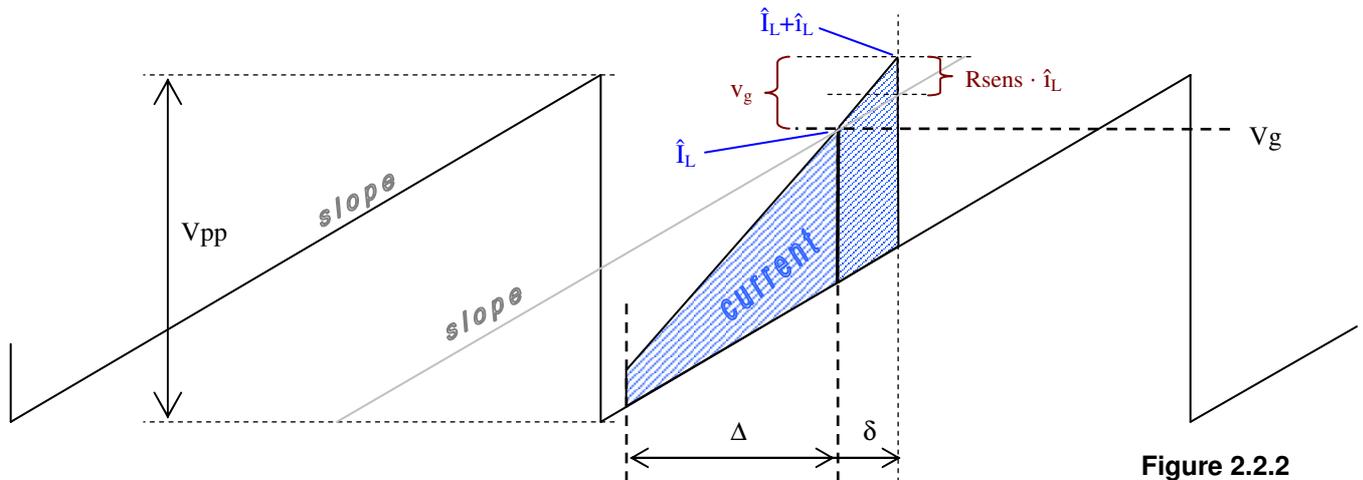


Figure 2.2.2

By studying figure 2.2.2 it is evident (after a little while) that

$$\delta \cdot V_{pp} + R_{sens} \cdot \hat{i}_L = v_g \quad \text{or} \quad \delta(s) = \frac{v_g(s) - R_{sens} \cdot \hat{i}_L(s)}{V_{pp}} \quad (2.2.1)$$

The left equation is verified by looking at the small triangles in the top of the picture.

If the compensation ramp is not linear for the whole switching period, V_{pp} should be replaced by the compensation slope at the switching instant multiplied by cycle time: $V_{pp} = \text{slope} \cdot T$.

(2.2.1) is one of the fundamental equations for current mode control with any amount of slope compensation, from pure CMC to pure DCC.

With CMC the duty cycle is a secondary parameter since the switch is not controlled by duty cycle but by current. The duty cycle is now a variable which depends on both peak current $R_{sens} \cdot \hat{i}_L(s)$ and control voltage $v_g(s)$. The relation between these three quantities is sometimes expressed by the so-called modulator gain:

$$\text{modulatorgain} = \frac{\delta(s)}{v_g(s) - R_{sens} \cdot \hat{i}_L(s)} = \frac{1}{V_{pp}} \quad \text{or} \quad R_{sens} \cdot \hat{i}_L(s) = v_g(s) - \delta(s) \cdot V_{pp} \quad (2.2.2)$$

A verbal interpretation of the modulator gain is: If the difference between control voltage and measured peak current $R_{sens} \cdot \hat{i}_L$ moves, how much does this affect the duty cycle? Answer: with a factor of $1/V_{pp}$.
 Another interpretation: peak current follows the control signal minus $V_{pp} \cdot$ duty cycle variations. If $V_{pp} = 0$, peak current follows control signal precisely.
 See a further discussion of the PWM modulator and its gain in appendix 1.

We should do a few checks to verify (2.2.1) in some simple special cases. The two cases which are simple are pure CMC and pure DCC:

If $R_{sens} = 0$ we have pure DCC and duty cycle in (2.2.1) will become $\delta(s) = \frac{v_g(s)}{V_{pp}}$ which is the well known PWM gain in Voltage Mode Control:

When V_g moves from ramp bottom to ramp top, Δ moves from 0 to 1, so $\frac{dV_g}{d\Delta} = \frac{V_{pp}}{1}$ or $d\Delta = \frac{dV_g}{V_{pp}}$

If $V_{pp} = 0$, the modulator gain goes to infinity, which can only be true if the denominator of (2.2.2) goes to zero, implying that $R_{sens} \cdot \hat{i}_L(s) = v_g(s)$.
 This is pure current mode control where the peak current follows the control signal. Also this result looks correct. $\delta(s)$ disappears from this equation, agreeing with the statement that pure current mode control does not care about duty cycle. There is a duty cycle of course and equation (2.1.8) and (2.1.9) must still be fulfilled, but δ is not a control variable any more.

2.3 Imperfections of peak current mode control

Observing figure 2.2.1 it is obvious that output voltage in a buck power stage must be determined by inductor current, or more precisely the average inductor current pr. cycle $I_L + i_L$.

On the other hand, the control mechanism in CMC controls peak current $\hat{I}_L + \hat{i}_L$, according to the modulator gain expressions. There are two things that can cause average current deviations i_L not to follow peak current deviations \hat{i}_L :

1. Average current is peak current minus half the peak-peak ripple current. Peak-peak current depends on V_i and V_o . So if V_o changes, average current will change without change of peak current.
2. Later we shall learn about subharmonic behaviour, which causes the average current pr. cycle to bounce forth and back after a step in peak current control.

What we must do is therefore, somehow, to replace \hat{i}_L with i_L in the modulator gain expression. If the modulator gain contains i_L , it will contain the same current variable as all other equations we write for the system, for instance (2.1.8), which enables us to solve them.

We start with the ripple current effect and leave the subharmonic effect till chapter 3.

2.4 Ripple current effect

The inductor current ripple current depends, among others, on the relation input / output voltage. Since output voltage and duty cycle are variable, the ripple current will be so too. The effect will be most visible at low frequencies, because an output capacitor will prevent output voltage from changing fast.

In most practical cases the ripple effect does not have significant influence on the performance of a feedback loop. But especially in cases where we use a low value output capacitor it causes a significant loss of low frequency gain. This normally does not affect loop stability which depends more on the gain at medium frequencies and how the gain passes through 0dB. But it can affect properties like input hum suppression.

The problem is this: The average inductor current I_L is not equal to peak current \hat{I}_L but peak current minus half of the peak-peak ripple current I_{pp} . This applies to inductor current pr. cycle at any moment:

$$I_L + i_L(s) = \hat{I}_L + \hat{i}_L(s) - \frac{1}{2} \cdot [I_{pp} + i_{pp}(s)] \quad (2.4.1)$$

Since the ripple current in the inductor depends on output voltage $V_o + v_o$ which is variable, i_L will be a function of both control voltage v_g and output voltage v_o .

Extracting small signal parts:
$$\hat{i}_L(s) = i_L(s) + \frac{1}{2} i_{pp}(s) \quad (2.4.2)$$

We proceed by expressing the inductor ripple current in terms of input and output voltage.

Law of inductors:
$$I_{pp} = \frac{V_i - V_o}{L} \cdot \Delta \cdot T = \frac{1}{F \cdot L} \cdot (V_i - V_o) \cdot \frac{V_o}{V_i} \quad (2.4.3)$$

Adding small signal terms to the two variables I_{pp} and V_o :

$$I_{pp} + i_{pp}(s) = \frac{1}{F \cdot L} \cdot [V_i - (V_o + v_o(s))] \cdot \frac{V_o + v_o(s)}{V_i} = \frac{1}{F \cdot L} \cdot \frac{V_i V_o + V_i v_o(s) - V_o^2 - 2 \cdot V_o \cdot v_o(s) - v_o(s)^2}{V_i} \quad (2.4.4)$$

Isolating small signal terms and neglecting the product of two small signal terms:

$$i_{pp}(s) = \frac{1}{F \cdot L} \cdot \frac{V_i - 2 \cdot V_o}{V_i} \cdot v_o(s) \quad (2.4.5)$$

Inserting (2.4.5) in (2.4.2) we get
$$\hat{i}_L(s) = i_L(s) + \frac{1}{2 \cdot F \cdot L} \cdot \frac{V_i - 2 \cdot V_o}{V_i} \cdot v_o(s) \quad (2.4.6)$$

and then inserting (2.4.6) in the modulator gain expression (2.2.1):

$$\delta(s) = \frac{v_g(s) - R_{sens} \cdot i_L(s) - \frac{R_{sens}}{2 \cdot F \cdot L} \cdot \frac{V_i - 2 \cdot V_o}{V_i} \cdot v_o(s)}{V_{pp}} \quad (2.4.7)$$

If we hide the Laplace operator (s) and re-arrange a bit we now get

$$\delta = \frac{1}{V_{pp}} \cdot v_g - \frac{R_{sens}}{V_{pp}} \cdot i_L - \frac{R_{sens}}{F \cdot L \cdot V_{pp}} \cdot \left(\frac{1}{2} - \frac{V_o}{V_i} \right) \cdot v_o \quad (2.4.8)$$

Now we are happy. This modulator gain expression contains i_L , not \hat{i}_L .

The last term is the correction term for ripple current effect. Note that if $V_o = \frac{1}{2} \cdot V_i$, i.e. $\Delta = 50\%$ (neglecting R_L) this term becomes zero.

2.5 Calculation of buck power gain

Equivalent to (2.1.8) we will now find a general expression for inductor current $i_L(s)$ versus control signal $v_g(s)$ which is valid for both CMC, DCC and any combination in between. The power gain of the power stage shall be defined as the ratio

$$\text{Powergain} = \frac{i_L(s)}{v_g(s)} \quad (2.5.1)$$

Hereafter the Laplace operator (s) will still be implied in the small signal variables but we will not write it, in order to increase clarity of the expressions. Let us now re-use figure 2.2.1:

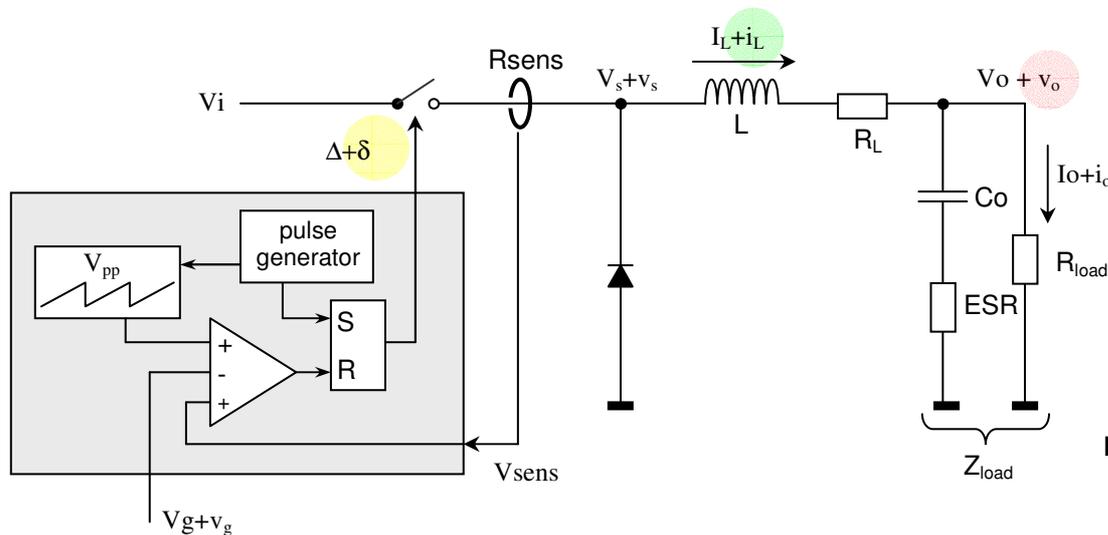


Figure 2.5.1

For simplicity let us write the inductor impedance as $Z_L = s \cdot L + R_L$

To find the Powergain we can use the following three equations with the unknowns δ , i_L and v_o .

$$\text{I} \quad \delta = v_g \cdot \frac{1}{V_{pp}} - \frac{i_L \cdot R_{sens}}{V_{pp}} - v_o \cdot \frac{R_{sens}}{F \cdot L \cdot V_{pp}} \cdot \left(\frac{1}{2} - \frac{V_o}{V_i} \right) \quad (2.5.2) = (2.4.7)$$

$$\text{II} \quad i_L = \delta \cdot \frac{V_i}{Z_L} - v_o \cdot \frac{1}{Z_L} \quad (2.5.3) = (2.1.7)$$

$$\text{III} \quad v_o = i_L \cdot Z_{load} \quad (2.5.4)$$

Eliminating δ and v_o from these equations leads to

$$\text{Powergain} = \frac{i_L}{v_g} = \frac{V_i}{V_{pp} \cdot (Z_L + Z_{load}) + V_i R_{sens} + \frac{R_{sens}}{F \cdot L} \cdot V_i \left(\frac{1}{2} - \frac{V_o}{V_i} \right) \cdot Z_{load}} \quad (2.5.5)$$

The last term in the denominator contains the ripple correction term.

$$K_{rip} = \frac{R_{sens}}{F \cdot L} \cdot V_i \left(\frac{1}{2} - \frac{V_o}{V_i} \right) \quad (2.5.6)$$

If you prefer the gain from v_g to v_o , which is perhaps more usual, here it is:

$$V_{\text{powergain}} = \frac{v_o}{v_g} = \text{Powergain} \cdot Z_{load} = \frac{V_i}{V_{pp} \cdot \left(\frac{Z_L}{Z_{load}} + 1 \right) + V_i \frac{R_{sens}}{Z_{load}} + \frac{R_{sens}}{F \cdot L} \cdot V_i \left(\frac{1}{2} - \frac{V_o}{V_i} \right)} \quad (2.5.7)$$

Z_{load} must include the output capacitor + any load connected to the output.

R_{load} is only equal to V_o/I_o for a resistive load. Generally R_{load} means the *dynamic* load connected to the output, i.e. v_o/i_o which is not necessarily equal to V_o/I_o .

(2.5.5) + (2.5.7) are ready-to-use equations for CCM that you can copy into a calculator and plot their gain and phase - see examples in chapter 3.10.

A little discussion of (2.5.5) and (2.5.6). You can skip this part if you are curious for the next chapter.

With pure **Duty Cycle Control** ($R_{sens} = 0$) the ripple factor disappears and (2.5.5) turns into

$$i_L(s) = \frac{v_g(s)}{V_{pp}} \cdot \frac{V_i}{Z_L + Z_{load}} = \frac{\delta(s) \cdot V_i}{Z_L + Z_{load}} \quad (2.5.8)$$

which seems correct. Compare to (2.1.8).

The ripple factor K_{rip} has effect only with Current Mode Control.

K_{rip} becomes zero if $V_i = 2 \cdot V_o$, i.e. if $\Delta = 50\%$. If $\Delta < 50\%$ K_{rip} is positive. If $\Delta > 50\%$ K_{rip} is negative.

So the ripple current has no effect on Powergain at the magic point $\Delta = 50\%$.

With pure **Current Mode Control** ($V_{pp} = 0$) (2.5.5) turns into

$$\text{Powergain} = \frac{i_L}{v_g} = \frac{1}{R_{sens} \cdot \left(1 + \frac{\frac{1}{2} - \frac{V_o}{V_i}}{F \cdot L} \cdot Z_{load} \right)} \quad (2.5.9)$$

We see here that when $V_o = \frac{1}{2} \cdot V_i$, Powergain is simply $1/R_{sens}$ as you would normally assume for pure CMC. This means that the power stage becomes a controlled current source, hence completely eliminating the 2nd order nature of a duty cycle controlled buck converter. This is an advantage in feedback loop design since it turns the normally complex double pole into a single real pole which originates in the output capacitor.

But when V_o is not $= \frac{1}{2} \cdot V_i$ we do not have a pure current source any more. In fact, if $V_o < \frac{1}{2} \cdot V_i$ the output current drops for constant v_g if V_o rises, and vice versa. This is equivalent to a power generator having a positive output resistance. And if $V_o > \frac{1}{2} \cdot V_i$ the opposite should happen – a power generator with a negative output resistance (!!)

This can also be understood from the fact that a buck converter has maximum ripple at $V_o = \frac{1}{2} \cdot V_i$. Investigating the derivative of (2.4.2) should show that. If the buck converter is controlled by a constant peak inductor current the average inductor current will be minimum when $V_o = \frac{1}{2} \cdot V_i$. When $V_o \neq \frac{1}{2} \cdot V_i$ the inductor current (= output current) will be higher.

(2.5.9) leads to a peculiar consequence. If we assume that the load impedance is a capacitor C_x , then for $V_o < \frac{1}{2} \cdot V_i$

$$\text{Powergain} = \frac{1}{R_{\text{sens}}} \cdot \frac{s}{s + \frac{1}{R_x C_x}} \qquad R_x = \frac{F \cdot L}{\frac{1}{2} - \frac{V_o}{V_i}} > 0 \qquad (2.5.10)$$

and for $V_o > \frac{1}{2} \cdot V_i$

$$\text{Powergain} = \frac{1}{R_{\text{sens}}} \cdot \frac{s}{s - \frac{1}{R_x C_x}} \qquad R_x = \frac{F \cdot L}{\frac{V_o}{V_i} - \frac{1}{2}} > 0 \qquad (2.5.11)$$

In both cases R_x is a fictitious positive resistance.

Powergain in (2.5.11) shows a Right Half Plane Pole on the x-axis which will become part of the open loop gain. If $V_o > \frac{1}{2} \cdot V_i$, the power stage gain will indeed be unstable – the duty cycle will either rush to 50% or 100% for constant control signal v_g .

But this discussion is a bit academic. We are going to see that a Current Mode Controlled buck stage in CCM will exhibit subharmonic oscillation if operated above 50% duty cycle. Subharmonic oscillation is normally not accepted and the cure for it is to introduce some slope compensation, by letting V_{pp} be > 0 .

Doing the calculations, it turns out that the necessary slope compensation to kill subharmonic oscillation is exactly what is required to turn the Right Half Plane Pole into a Left Half Plane Pole in the above equations. Nature is really well thought out 😊

If, however, we operate the converter in DCM with $V_o > \frac{1}{2} \cdot V_i$, the subharmonic behaviour is absent, we don't have to apply slope compensation, and the power stage is indeed unstable at DC and will tilt, if the feedback is removed and V_g is left constant.

But in a closed loop this does not necessarily mean an unstable system. Since this kind of instability of the buck stage at $V_o > \frac{1}{2} \cdot V_i$ shows itself at DC and low frequencies, a closed and normally fast feedback loop should easily be able to correct for it. A peculiar detail which not many know about.

Compare it with a cyclist. As long as he is riding, he is able to correct errors in balance by regulating the handlebar. He is part of a fast acting feedback system. But if he stops riding, regulating the handlebar will not have any effect, and he will tilt to one side or the other because a bicycle with only two wheels is unstable.

2.6 Completing the loop

The total open loop gain of a buck converter is $A_o = \text{Powergain} \cdot Z_{\text{load}} \cdot \text{Gain}_g$. $\text{Gain}_g(s)$ is the frequency dependent feedback gain as shown in the closed loop model in figure 4.5.2. The feedback path typically comprises one or several amplifier stages with local feedback and resistive or resistive + capacitive voltage dividers. An opto coupler or a transconductance amplifier can also be part of the feedback path.

For stability the open loop gain versus frequency must be controlled so that there is a reasonable phase- and gain margin. Good rules of thumb tell us to keep a phase margin of at least 45 degrees and a gain margin no less than 6 – 10 dB. This is normally achieved by adjusting poles and zeros in the frequency dependent error amplifier gain which is part of Gain_g - a process normally called 'compensating the error amplifier'. Describing the gain of this part is well-known craftsmanship for most engineers and will not be part of this article.

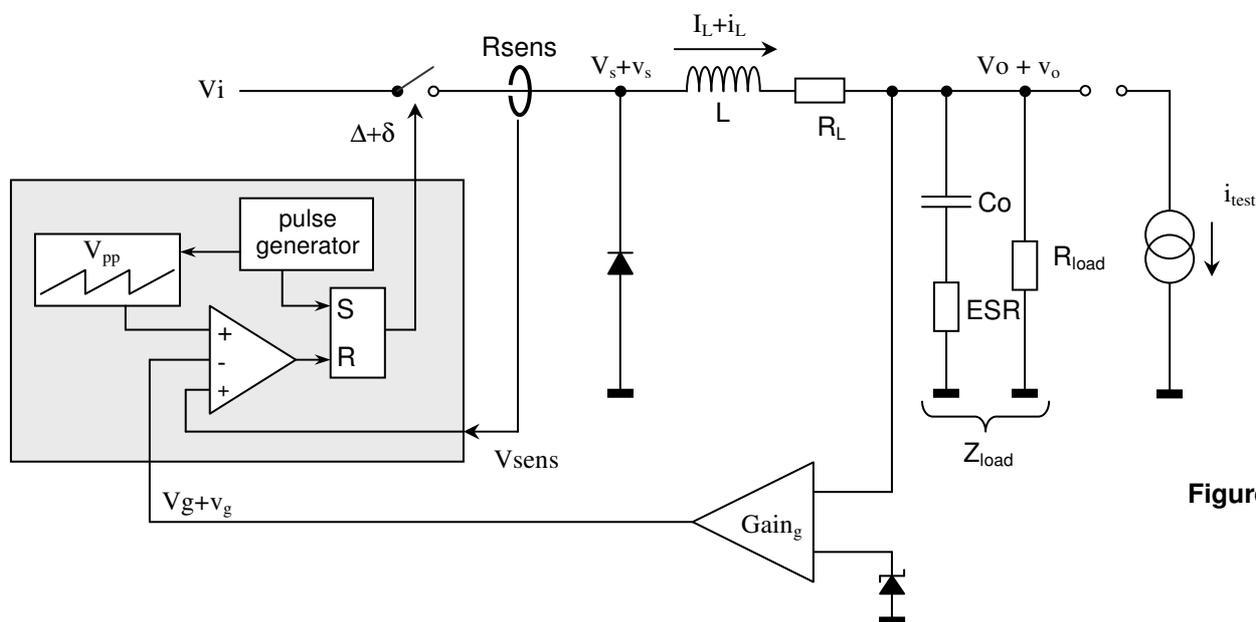


Figure 4.5.2

3 Including subharmonic behaviour

The intrinsic subharmonic instability of a peak Current Mode Controlled power stage in CCM has been known for many years. With pure CMC (no slope compensation) such a power stage becomes unstable and starts self oscillating at half the switching frequency ($F/2$) when the duty cycle Δ exceeds 50%, even without any external feedback loop. The subharmonic behaviour is an inherent property of a peak current controlled power cell.

Does this mean that a current controlled power cell running at $\Delta < 50\%$ is always stable? Yes, in itself it will not oscillate, but close to 50% duty cycle it will still behave as if it had a resonance at $F/2$. A resonance whose Q goes towards infinity when Δ approaches 50%. After a step command the inductor current will bounce in steps around the new value with an alternating current error decreasing exponentially in time. A kind of 'digital' or 'sampled' ringing.

So even though the power cell itself does not oscillate, the apparent resonance at $F/2$ can cause an outer voltage feedback loop to become unstable at $F/2$, if the gain peak at $F/2$ is not sufficiently suppressed.

This effect was not covered in my loop calculators until now.

Dr. Ray Ridley investigated the subharmonic phenomenon many years ago in his ground-breaking PHD dissertation (ref. 3) and published equations to describe it and its influence in an outer voltage loop. However, when I try to apply those equations in a calculator, I find areas where the results are incorrect. The same seems to apply to others who use them, including dr. Ridley himself (ref. 6).

The published data also does not provide much understanding to the reader of the physics behind the equations. Or perhaps I am just not skilled enough to handle the information.

For some years I have therefore been dreaming of building up my own understanding and incorporating the subresonance phenomenon in my loop calculators. My feeling was that once a good mathematical description was made, it would be simple to implement it in the present calculators as a small addition without changing all the present equations.

The obstacle was that a subresonance ringing should best be described with math for sampled data, which is more or less unfamiliar to me and many of my fellow analog engineers. I think we all learned about Z-transform at the engineering school, but not many have used it since school time.

It would be a natural approach for an analog engineer to see the power cell with analog eyes and describe its behaviour with the more familiar 2nd order transfer function with a resonance at $F/2$ and a Q fitting with the exponential decay of a current error. In other words, replace the 'sampled' step-ringing with an analog one with an exponentially decaying sine shaped disturbance. This is apparently what was done in (ref. 3+6+8), but it is not clear how the equations were derived or when or when not to use them.

During 2017 - 18 my dream started to crystallize into specific results, and indeed the subharmonic behaviour can be modelled and included by basically replacing one simple equation with another. However, the derivation of that equations takes a lot of explanation.

In the present article I will try to let you look into the theory or the theories that I found useful. In fact I tried both the analog and the digital – or sampled – approach. It turns out that the analog approach evolves into heavy equation work, whereas the sampled approach looks much simpler, albeit with a strange looking result which does not appeal much to an analog mind. Therefore I will also go through some essential sampled data analysis concepts that are useful in the derivation.

Both methods rely heavily on Laplace transforms. My admiration for Mr. Laplace keeps rising.

A peak current controlled power cell can be seen as an inner current loop with its own open loop gain and phase. Many papers deal with it as a separate inner loop whose closed loop gain is i_L/v_g i.e. the small signal deviations of inductor current versus control voltage, as in figure 2.2.1 for instance. We need to know i_L/v_g to calculate an outer voltage loop.

It can be explained that when duty cycle Δ comes close to 50%, the gain margin of the inner current loop approaches 0 dB while phase lag is 180 degrees at $F/2$, therefore the closed current loop shows a gain peak and will ring at $F/2$.

There has been a lot of controversy about this inner current loop and the way to understand it correctly (ref. 9) The modulator gain discussion in appendix 1 fits nicely into that story.

I don't think it is necessary to open the inner current loop and discuss its strange properties, since it is the closed loop gain i_L/v_g or the transconductance of the power cell we need to care about. In a buck converter we have earlier used the name 'Powergain' for i_L/v_g (but differently in boost and buck-boost).

It is possible to describe the closed loop behaviour without considering it a loop at all. At least according to my view, some others would probably disagree with me.

In the next chapters we shall see how it can be done.

3.1 What do subharmonics look like?

Figure 3.1.1 is nearly the same as figure 2.2.1 - a buck converter with a current controlled power cell. Let us first see how it works without slope compensation, i.e. with $V_{pp} = 0$ where the peak inductor current is exactly set by the programming signal V_g . The switch is turned on by a clock signal and turned off when the set current is reached in each pulse. The control signal only controls peak current. It has no influence on what happens to the current between the peaks or when the peaks occur.

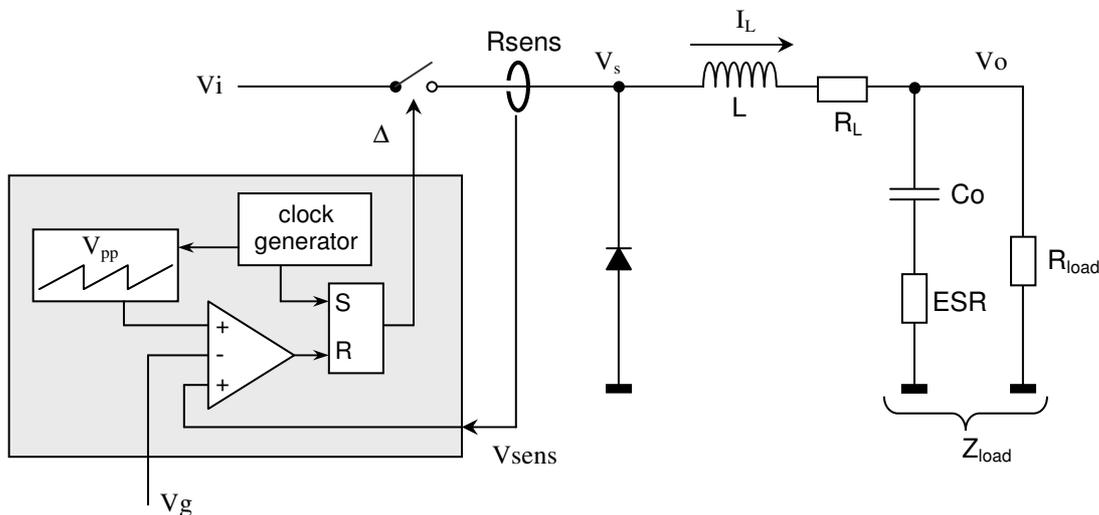


Figure 3.1.1

Figure 3.1.2 is an example showing how the inductor current I_L moves from one steady state to a higher one after a step in the control signal. In this case duty cycle Δ is close to 40%. We see that the current does not hit its new steady state immediately. There is a current error starting to be equal to the step size and then bouncing forth and back with an exponentially decaying error.

Thus, by simply drawing a few lines on a piece of paper, the sampled ringing at $F/2$ appears immediately. The error shifts sign for each pulse while decaying exponentially. We just need to express it in an equation.

We are assuming that slopes are constant, i.e. input and output voltages do not move while the bouncing dies out.

Note that the "sampling" instants are at the instants of peak current, not the clock signal.

What would happen if Δ was not 40% but 60%?

As an exception, waste a piece of paper by printing out figure 3.1.2, go to the bathroom and look at it in the mirror to reverse the x-axis. Now you see 60% duty cycle and a small start error exponentially rising while bouncing around the intended steady state. This is what we call subharmonic oscillation in the power cell when $\Delta > 50\%$.

Maybe we should clarify what we mean with duty cycle Δ . This may become unclear if we replace the diode with another active switch or if we want to create an 'inverse peak current mode' control where we turn off the active switch when the bottom (negative peak) current hits a programming signal. This is possible but never really used.

Δ is always the relative length of the time period following immediately after the clock signal.

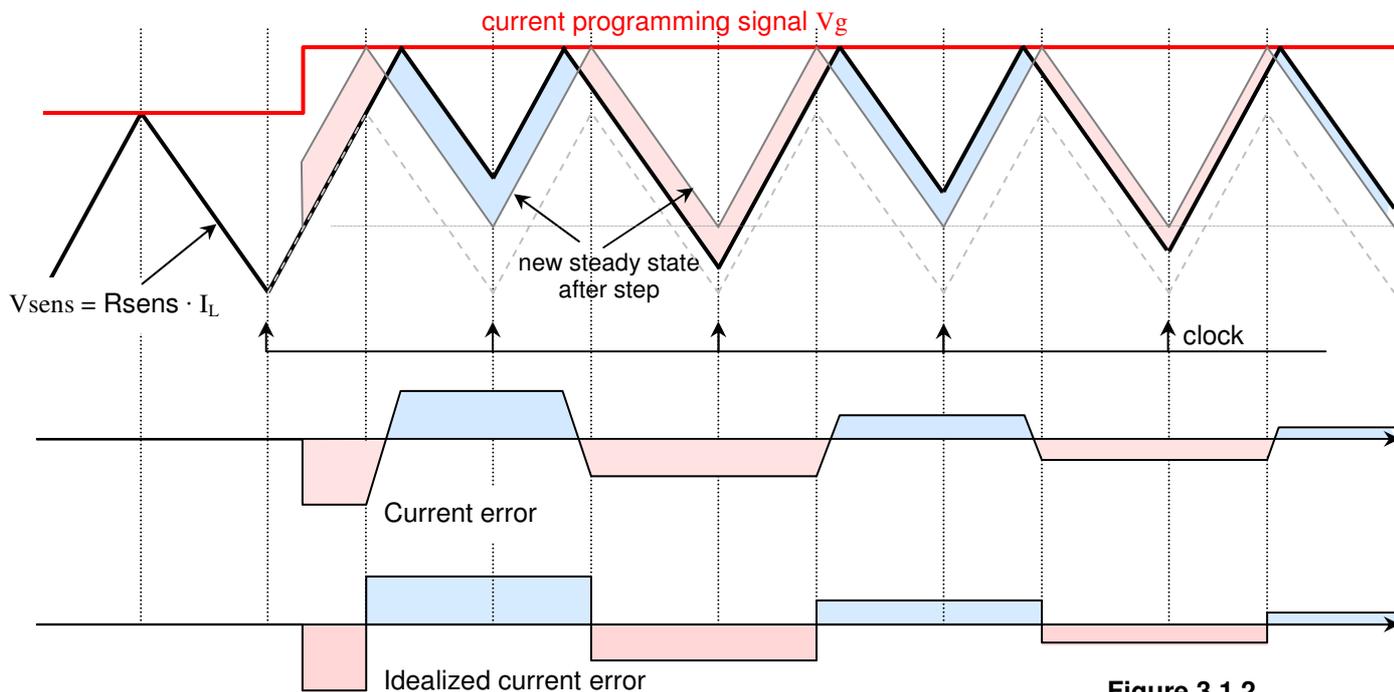


Figure 3.1.2

The decay of the current error will depend on duty cycle Δ . Close to 50% the decay pr. cycle is low, and the sampled ringing takes a long time to vanish. At low Δ the error vanishes within a few cycles. Let us define a factor "pro" as the error in one cycle relative to the error in the previous cycle. In the example above "pro" will be close to $-0,7$. It is negative when the error shifts sign each cycle and positive if the error has the same sign as in the previous cycle.

3.2 The progression factor 'pro'

The next step is to find "pro". With no slope compensation it is easy.

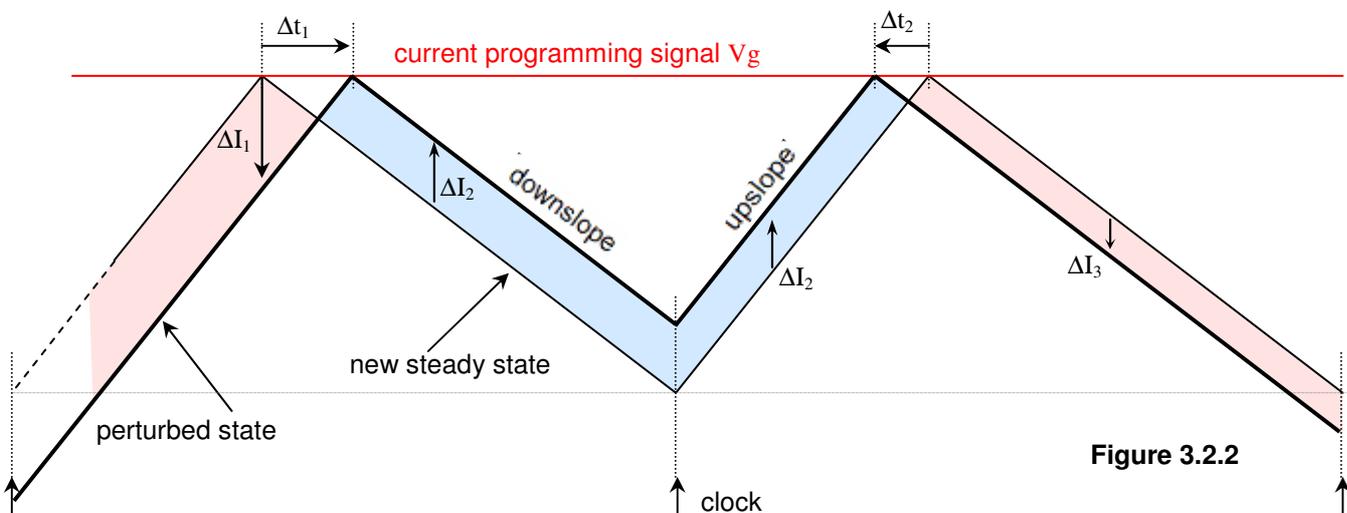


Figure 3.2.2

The slopes of the sensed inductor current are called 'upslope' and 'downslope'. Both are defined as positive numbers.

By simple geometric observation in figure 3.2.2 the following relations can be written:

$$\Delta t_1 = \frac{-\Delta I_1}{\text{upslope}} \quad \Delta I_2 = \Delta t_1 \cdot \text{downslope} \quad \Delta I_2 = -\Delta I_1 \cdot \frac{\text{downslope}}{\text{upslope}}$$

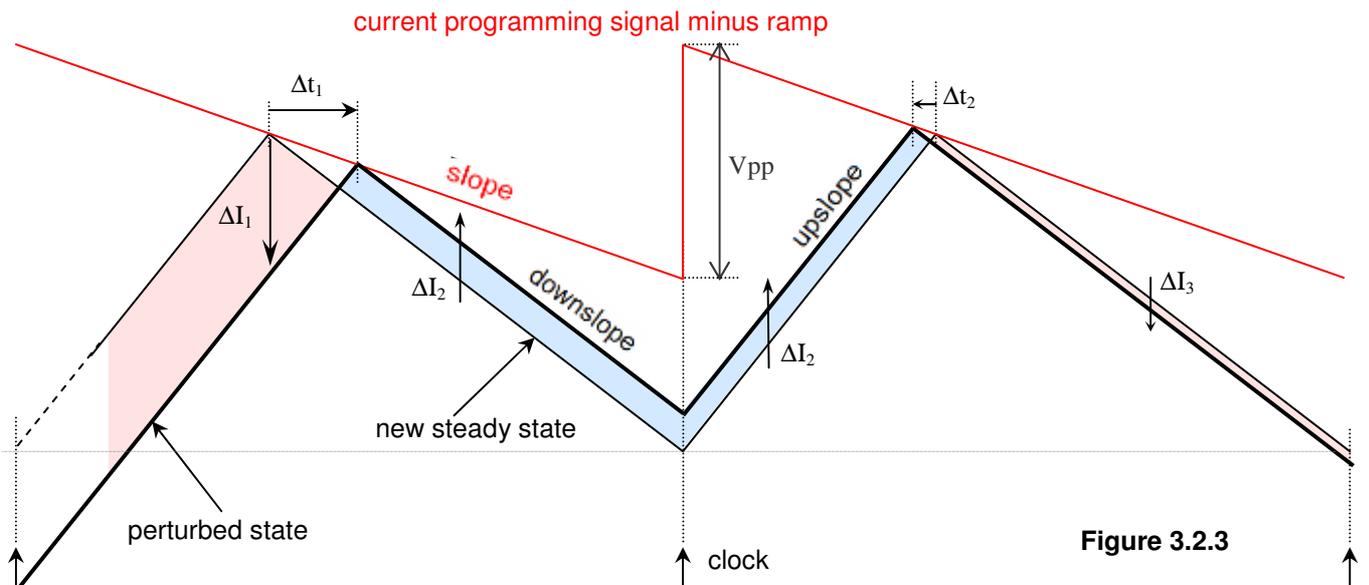
$$\text{pro} = \frac{\Delta I_2}{\Delta I_1} = \frac{-\text{downslope}}{\text{upslope}} \quad (3.2.1)$$

The same ratio would be found for $\frac{\Delta I_3}{\Delta I_2}$, $\frac{\Delta I_4}{\Delta I_3}$, etc.

As expected, if $\Delta = 50\%$ $\text{downslope} = \text{upslope}$, therefore $\text{pro} = -1$ which means the sampled ringing will never die out.

Now we shall see what happens when we add slope compensation. In figure 2.2.2 we showed the slope ramp V_{pp} added to the sensed inductor current, the sum compared to a fixed programming signal V_g . This is what most current mode control ICs do.

But we can just as well subtract the slope ramp from the programming signal and compare the difference with sensed current. In the following drawings we will do that. In this way the consequences may be easier to see.



With the same method as before we will find $\text{pro} = \frac{\Delta I_2}{\Delta I_1}$. All three slopes are defined as positive numbers.

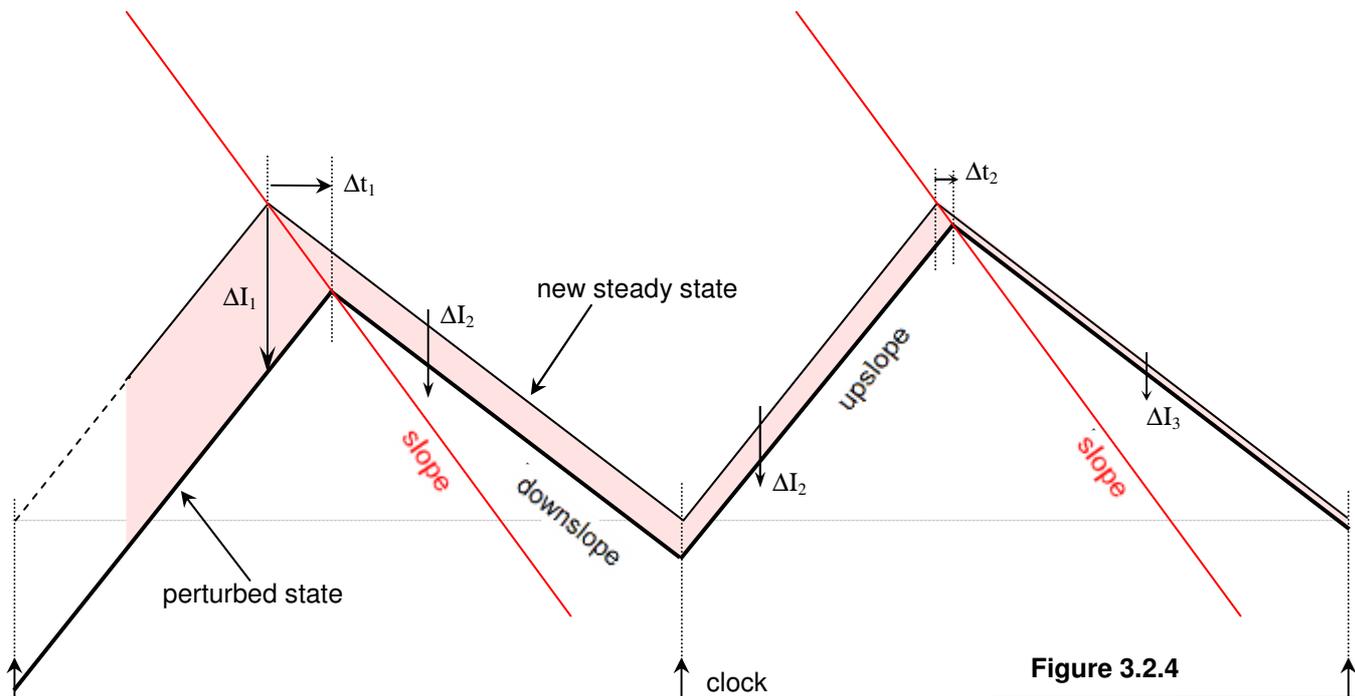
$$\Delta t_1 = \frac{-\Delta I_1}{\text{upslope} + \text{slope}} \quad \Delta I_2 = \Delta t_1 \cdot (\text{downslope} - \text{slope}) \quad \Delta I_2 = -\Delta I_1 \cdot \frac{\text{downslope} - \text{slope}}{\text{upslope} + \text{slope}}$$

$$\text{pro} = \frac{\Delta I_2}{\Delta I_1} = \frac{\text{slope} - \text{downslope}}{\text{slope} + \text{upslope}} \quad (3.2.2)$$

You may have to scratch your hair a few times to verify these simple relations. Fortunately, everyone seems to agree on them.

If $\text{slope} = \text{downslope}$, ΔI_2 and pro become zero. It is evident from figure 3.2.3 that if slope and downslope are equal, any current error will be gone after the first current peak. This means that the steady state will be reached within one cycle.

We must also show the picture if slope > downslope.



Geometric observations in triangles drawn around the peak current show that equation (3.2.2) is still valid, but since slope > downslope, p_{ro} becomes > 0.

There is no ringing left, only an exponentially decaying current error with constant polarity.

As we approach DCC, the sensed current slopes become insignificant, and p_{ro} should approach +1, meaning that a current error should persist for ever. This is mostly an academic viewpoint in a normal power supply. A permanent current error would make the output voltage rise and slopes change which will of course be corrected by an outer feedback loop. But if we are making a battery charger, where the load is an ideal battery, the statement is true. You cannot regulate a battery charger properly without involving current in the regulation.

It is interesting that we did not have to refer to any specific topology of the three basic PWM converter types while evaluating the progression factor. The equations for p_{ro} are true for all of them: buck, boost, and buck-boost.

3.3 Subharmonic modelling methods

The progression factor p_{ro} is an important factor for modelling, no matter what kind of model we choose. The most popular kind of model seems to be an analog equivalent 2nd order low pass filter circuit whose Q factor gives the same exponential decay of an analog ringing as the p_{ro} factor does on the sampled ringing. Ridley (ref 3) uses this approach, but after studying his literature many times the details of his modelling remain unclear to me.

In the next pages we shall see a more direct approach based on sampling theory, but probably less intuitive. It is based on the definitions in the Laplace transform. Because most of us have probably forgotten these definitions and their consequences, I will try to revive the basic concepts of the Laplace transform that we need to understand in order to build the model.

In chapter 3.8 I will also show you a way to build an equivalent model using an analog 2nd order low pass filter analogy. It turns out to be more complicated than the sampled analogy.

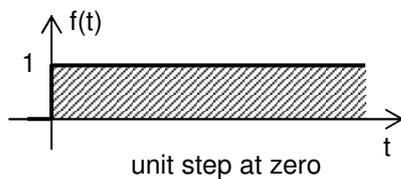
3.4 Laplace sampling gym

The Laplace transform is a mathematical manipulation of a time dependent signal, and the result is a mathematical expression of the same signal in terms of a complex frequency 's'. It has similarities to the Fourier transform but contains more information.

The frequency 's' is a complex number with a real part σ and an imaginary part $j\omega$: $s = \sigma + j\omega$ where $\omega = 2\pi \cdot \text{frequency}$ is the radial frequency. For a function $f(t)$ the Laplace transform is defined as

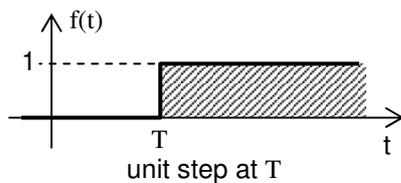
$$\text{Laplace}(f(t)) = f(s) = \int_0^{\infty} f(t) \cdot e^{-s \cdot t} dt \quad (3.4.1)$$

For sampled systems the function $f(t)$ is normally constant within the sampling period (switching period) T . This is convenient because it makes it very simple to write the Laplace transforms related to it. Let's see some useful examples:



$$f(t) = u(t)$$

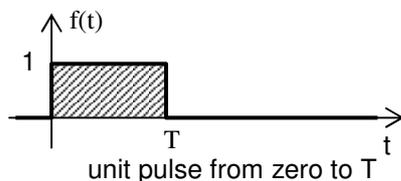
$$f(s) = \int_0^{\infty} e^{-s \cdot t} dt = -\frac{1}{s} \cdot (e^{-s \cdot \infty} - e^0) = -\frac{1}{s}(0 - 1) = \frac{1}{s} \quad (3.4.2)$$



$$f(t) = u(t - T)$$

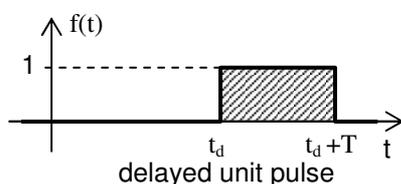
$$f(s) = \int_T^{\infty} e^{-s \cdot t} dt = -\frac{1}{s} \cdot (e^{-s \cdot \infty} - e^{-s \cdot T}) = -\frac{1}{s}(0 - e^{-s \cdot T}) = \frac{1}{s} \cdot e^{-s \cdot T} \quad (3.4.3)$$

Here we see that a delay of T multiplies $f(s)$ with e^{-sT} . The next case is the difference between the two first.



$$f(t) = u(t) - u(t - T)$$

$$f(s) = \frac{1}{s} - \frac{e^{-s \cdot T}}{s} = \frac{1}{s} (1 - e^{-s \cdot T}) \quad (3.4.4)$$



$$f(s) = \frac{1}{s} (1 - e^{-s \cdot T}) \cdot e^{-s \cdot t_d} \quad (3.4.5)$$

The equation (3.4.4) is also the transfer function of the 'hold' part of a normal sample & hold network. One way to explain that is that the rectangular pulse next to (3.4.4) is pr. definition the impulse response of a hold network: A dirac impulse with area = 1 on the input of a hold network makes it respond with the value '1' during one sampling time. A system's transfer function is generally identical to the Laplace transform of its impulse response, which is easily proven from the definition of the Laplace transform.

The transfer function known for a sample & hold network is very similar:

$$\text{SH}(s) = \frac{1}{s \cdot T} (1 - e^{-s \cdot T}) \quad (3.4.6)$$

Perhaps you remember that the output of a sampling process (without 'hold') contains the full spectrum of the original signal plus the same spectrum centred around all positive and negative harmonics of the sampling frequency. Therefore, the sampling transfer function (gain) is constant up to $F/2$.

The sampling only adds a division by T because the transfer function of the sampling process is 1/T up to half the sampling frequency.

A short explanation for the 1/T factor: If a signal has the value $x(nT)$ at time nT , then the area covered by the signal during the sample period from nT to $(n+1)T$ is $T \cdot x(nT)$, whereas the area in the corresponding sampling impulse is only $1 \cdot x(nT)$, because the dirac impulse defining sampling has an area of 1.

In fact we do not need to study the sample & hold process to reach our goal. I do it because it can give us some additional useful insight. Let us for instance plot the gain and phase of the sample & hold transfer function and see what it looks like.

As taught in literature on sampling theory there is a frequency dependent gain in the S&H process. At $F/2$ the gain is -4 dB.

The phase shift is the same as for a delay of $T/2$.

Mathcad has no problem in evaluating and plotting expressions in s for $s = j\omega$ like (3.4.6), but we may have. It can be instructive to open the Laplace expression and see what a sample & hold circuit really contains.

First a little manipulation:

$$SH(s) = \frac{1 - e^{-s \cdot T}}{s \cdot T} = \frac{e^{-s \cdot \frac{T}{2}} \left(e^{s \cdot \frac{T}{2}} - e^{-s \cdot \frac{T}{2}} \right)}{s \cdot T}$$

Then replace s with $j\omega$ to be able to plot it in a frequency plot:

$$SH(j \cdot \omega) = \frac{e^{-j \cdot \omega \cdot \frac{T}{2}} \left(e^{j \cdot \omega \cdot \frac{T}{2}} - e^{-j \cdot \omega \cdot \frac{T}{2}} \right)}{j \cdot \omega \cdot T} = e^{-j \cdot \omega \cdot \frac{T}{2}} \cdot \left(\frac{\sin\left(\omega \cdot \frac{T}{2}\right)}{\omega \cdot \frac{T}{2}} \right) \quad (3.4.7)$$

We have used Euler's equation:

$$\sin(x) = \frac{e^{j \cdot x} - e^{-j \cdot x}}{2j} \quad (3.4.8)$$

The first factor in (3.4.7) is a delay of $T/2 =$ half the sampling time.

The second factor is the well known sinc function $\sin(x)/x$ which has its first zero at $\omega = 2\pi \cdot F =$ the sampling frequency. The delay causes a phase lag increasing linearly with frequency, and the amplitude of the sinc function is the red curve in the upper part of figure 3.4.1.

Then how does the sample & hold function react on a step in the time domain?

Figure 3.4.2 shows the answer. The S&H response and the delay response are plotted by summing a lot of harmonics of a sampled & held square wave. It's the same method that I use to plot the step load response in my loop calculators.

Indeed the sampling process has an average delay = $T/2$, however with slopes ramping up or down with a slope duration of one sampling period. This is because the sampling instants are randomly related to the signal steps. One sampling period after a step all steps will be registered. Half a sampling period after a step only half of the steps have been registered. Therefore in average the response after $T/2$ is 0,5, etc.

What a fascinating revelation coming out of some Laplace exercises 😊

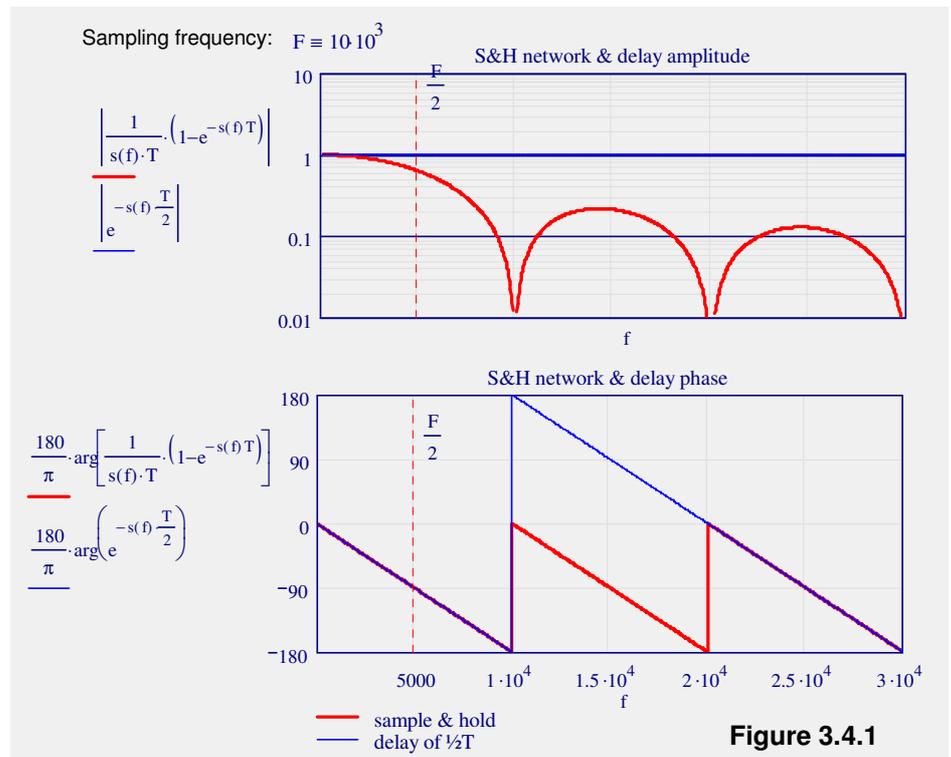


Figure 3.4.1

Sampling frequency: $F \equiv 10 \cdot 10^3$ [Hz]
 Test frequency: $F_o \equiv 1000$ [Hz]
 Input step: $I_{step} \equiv 1$

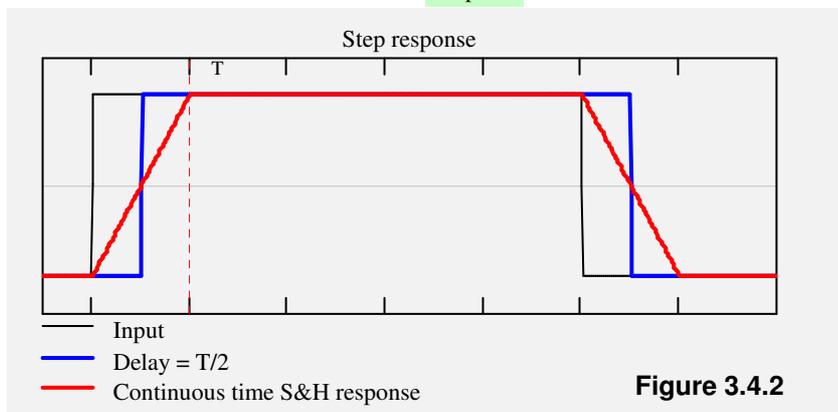


Figure 3.4.2

If we draw a sine wave with its sampled representation like in figure 3.4.3, the delay of T/2 is evident.

If we study the same signals on an oscilloscope and let the scope calculate the average of a lot of sweeps, we would also see an average sampled signal as a delayed sine with slightly lower amplitude than the original sine wave. This amplitude reduction will approach -4dB as the sine wave frequency approaches F/2.

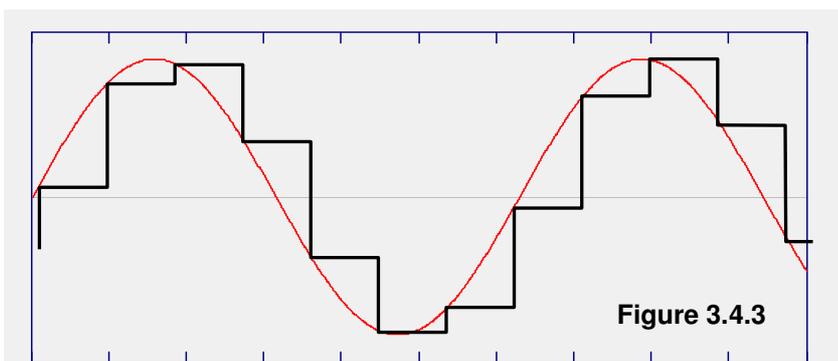


Figure 3.4.3

3.5 Subharmonics in Laplace domain

We are going to see that many things in subharmonic modelling show resemblance to what we just learned about sample & hold circuits. Let us first find the properties of a sampled ringing describing a current error as shown in figure 3.5.1.

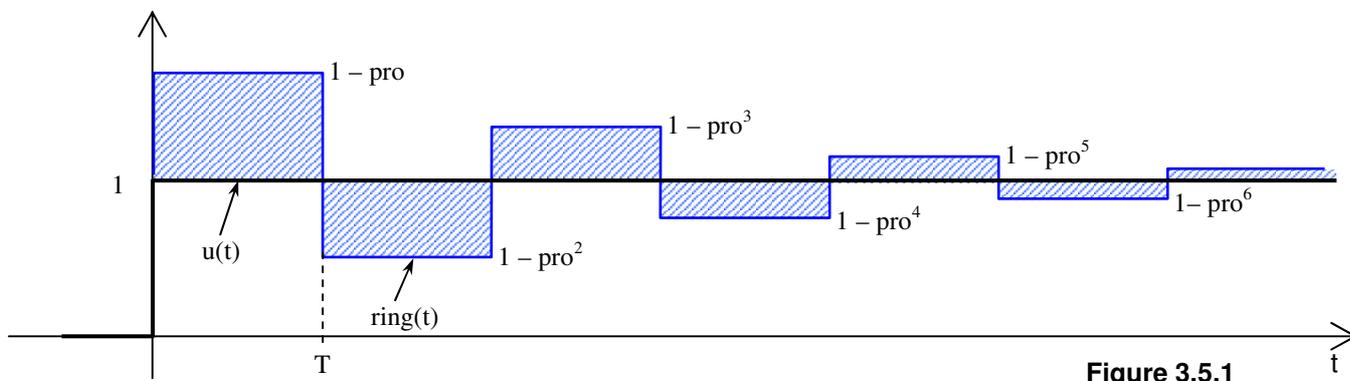


Figure 3.5.1

ring(t) represents a ringing current error like the idealized current error found in figure 3.1.2. In the ringing case pro is a negative number: here it is about -0,65. For each ringing half cycle the remaining current error is multiplied with pro, therefore the error values $1 - pro^N$ can be written on each half cycle.

The response can be described as a sequence of unit pulses scaled with pro^N :

$$\begin{aligned}
 \text{ring}(t) = & u(t) - \text{pro} \cdot (u(t) - u(t - T)) \\
 & - \text{pro}^2 \cdot (u(t - T) - u(t - 2 \cdot T)) \\
 & - \text{pro}^3 \cdot (u(t - 2 \cdot T) - u(t - 3 \cdot T)) \\
 & - \text{pro}^4 \cdot (u(t - 3 \cdot T) - u(t - 4 \cdot T)) \\
 & - \dots
 \end{aligned} \tag{3.5.1}$$

The Laplace transform is the sum of the transforms of all those unit pulses.
 Using the result from (3.4.5):

$$\begin{aligned}
 \text{ring}(s) = & \frac{1}{s} - \text{pro} \cdot \frac{1}{s} \cdot (1 - e^{-sT}) \\
 & - \text{pro}^2 \cdot \frac{1}{s} \cdot (1 - e^{-sT}) \cdot e^{-sT} \\
 & - \text{pro}^3 \cdot \frac{1}{s} \cdot (1 - e^{-sT}) \cdot e^{-s \cdot 2T} \\
 & - \text{pro}^4 \cdot \frac{1}{s} \cdot (1 - e^{-sT}) \cdot e^{-s \cdot 3T} \\
 & - \dots
 \end{aligned} \tag{3.5.2}$$

$$\text{ring}(s) = \frac{1}{s} - \frac{1}{s} \cdot \text{pro} \cdot (1 - e^{-sT}) \cdot (1 + \text{pro} \cdot e^{-sT} + \text{pro}^2 \cdot e^{-2 \cdot sT} + \text{pro}^3 \cdot e^{-3 \cdot sT} + \text{pro}^4 \cdot e^{-4 \cdot sT} + \dots) \tag{3.5.3}$$

Setting $x = \text{pro} \cdot e^{-sT}$ we can simplify: $\text{ring}(s) = \frac{1}{s} - \frac{1}{s} \cdot \text{pro} \cdot (1 - e^{-sT}) \cdot (1 + x + x^2 + x^3 + x^4 + \dots)$ (3.5.4)

The geometric series $1 + x + x^2 + x^3 + x^4 + \dots = \frac{1}{1 - x}$ for $|x| < 1$ according to mathematical handbooks.

Therefore we can simplify more: $\text{ring}(s) = \frac{1}{s} - \frac{1}{s} \cdot \frac{\text{pro} \cdot (1 - e^{-sT})}{1 - \text{pro} \cdot e^{-sT}}$ (3.5.5)

This is the Laplace transform of the unit step response $\text{ring}(t)$.

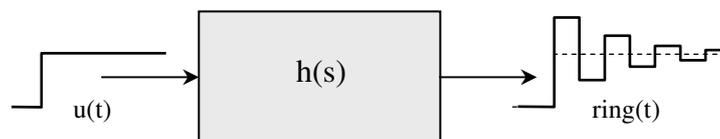


Figure 3.5.2

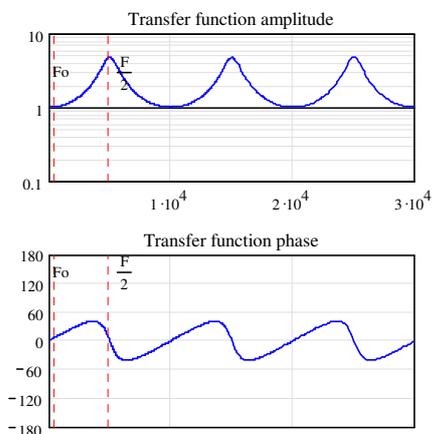
To find the transfer function $h(s)$ of a system having $\text{ring}(t)$ as its unit step response we can use the same system's response to a unit dirac impulse. Elementary Laplace rules say that $h(s) = \text{Laplace}(\text{dirac impulse response})$ which is also $= s \cdot \text{Laplace}(\text{unit step response})$.

So the system's transfer function will be

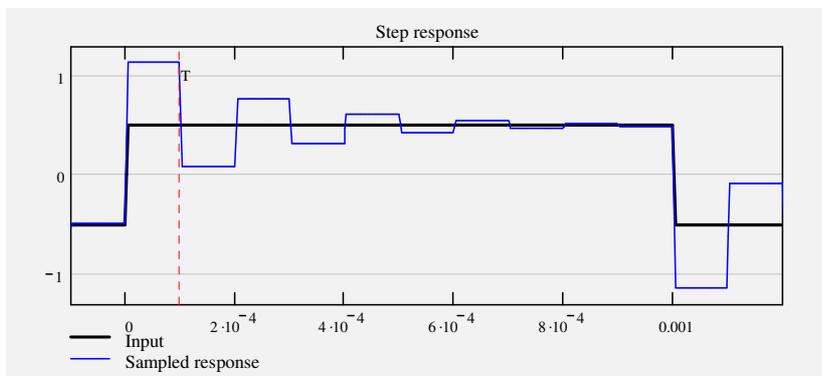
$$h(s) = s \cdot \text{ring}(s) = 1 - \frac{\text{pro} \cdot (1 - e^{-sT})}{1 - \text{pro} \cdot e^{-sT}} = \frac{1 - \text{pro}}{1 - \text{pro} \cdot e^{-sT}} \tag{3.5.6}$$

For $\text{pro} = 0$, $h(s) = 1$.

Let's plot $h(s)$ and its step response for $F = 10\text{kHz}$:

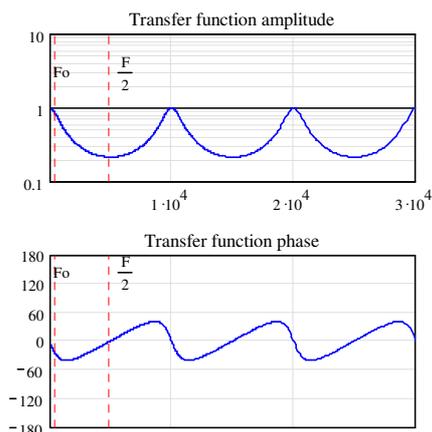


pro = -0.65

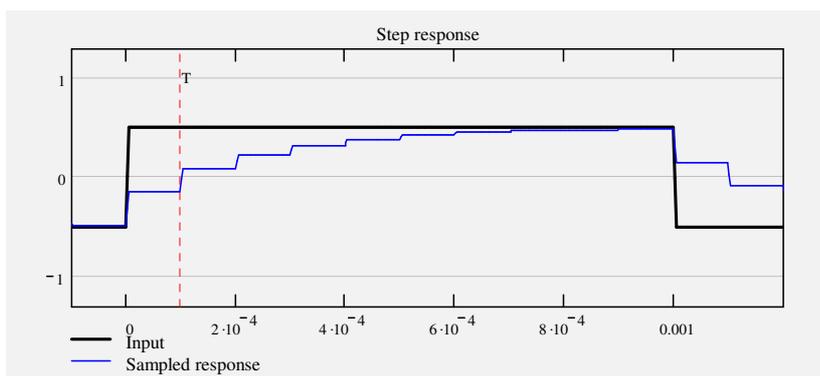


Fantastic. The step response is the best check that we have done the right calculations.

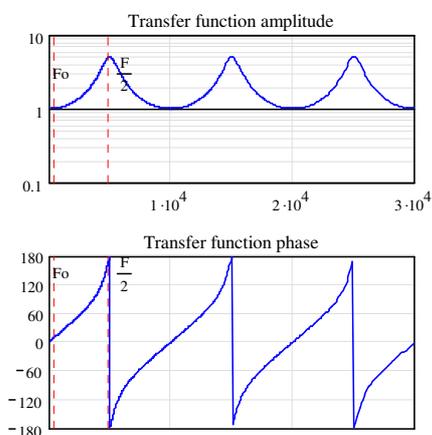
Some other examples. First an over damped system like the one in figure 3.2.4. $pro > 0$:



pro = 0.65



And what if the system is self oscillating: $pro < -1$:



pro = -1.5

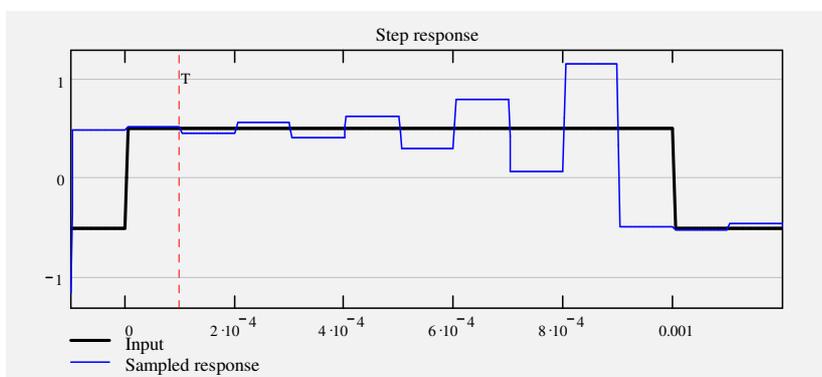


Figure 19.6.3

The equation (3.5.6) still works for $pro < -1$. We see an exponentially growing oscillation. The math handbooks set the restriction $|x| < 1$ for the geometric series $1 + x + x^2 + x^3 + \dots$ to have a valid result. But it seems it also gives meaningful results for other x . Maybe a mathematician can explain that.

3.6 A more accurate model of reality

The results of the previous chapter look very convincing, don't they?

But they are not showing exactly what a real current mode controlled circuit does. Reality is a little more subtle.

Two spooky things about $h(s)$ is that it can have a phase lead, and it has always a gain of 1 at the switching frequency. From sampling theory we remember that the gain at the sampling frequency should be 0, like in figure 3.4.1.

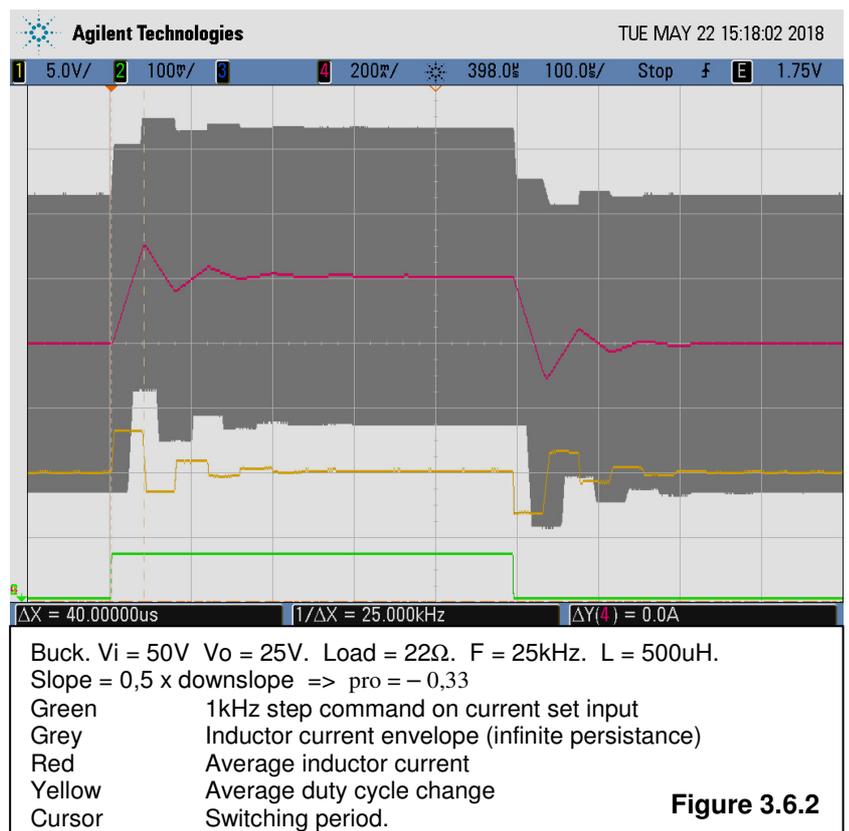
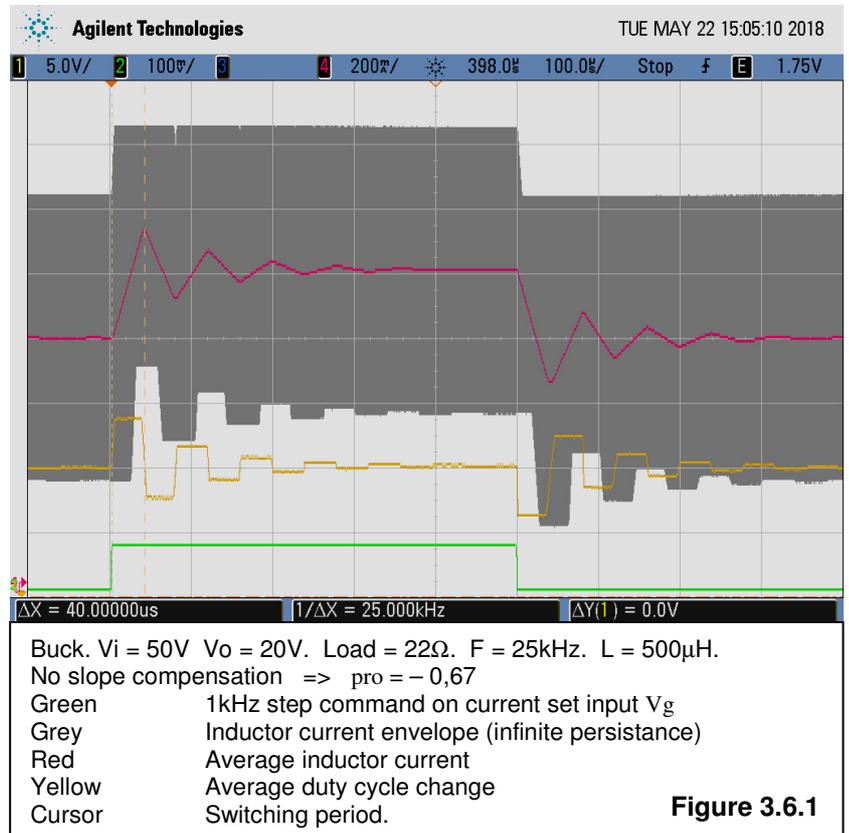
To see what the real world does, a buck test circuit was built equivalent to figure 3.1.1, a step command was injected on its V_g input. Inductor current was monitored on an oscilloscope – figure 3.6.1 - 3.6.4.

In the first experiment there is no slope compensation. Therefore the top envelope (peak) of the inductor current follows the control signal precisely. The sampled oscillation is only seen in the bottom envelope. The vertical width of the envelope is the peak-peak inductor current.

The average behaviour through hundreds of steps, shown in red, is a ringing triangle, not a ringing square wave.

The average duty cycle (average of switching node voltage) moves like a square wave ringing found by differentiating the average inductor current. This seems to make sense.

The second experiment was done with a moderate slope compensation added. Note that the ringing is better damped, even though duty cycle is now at 50%. Also note that the peak inductor current does no longer follow the control signal (top envelope).



In the third experiment we use slope compensation with slope = sensed inductor current downslope.

As predicted, the oscillation is gone. The response is the fastest possible, in average looking precisely like that of a sample & hold network – see figure 3.4.2.

In the fourth experiment we use much more slope compensation. In fact this is more like DCC with a control ramp (the slope), however with a small amount of current signal injected in the modulator.

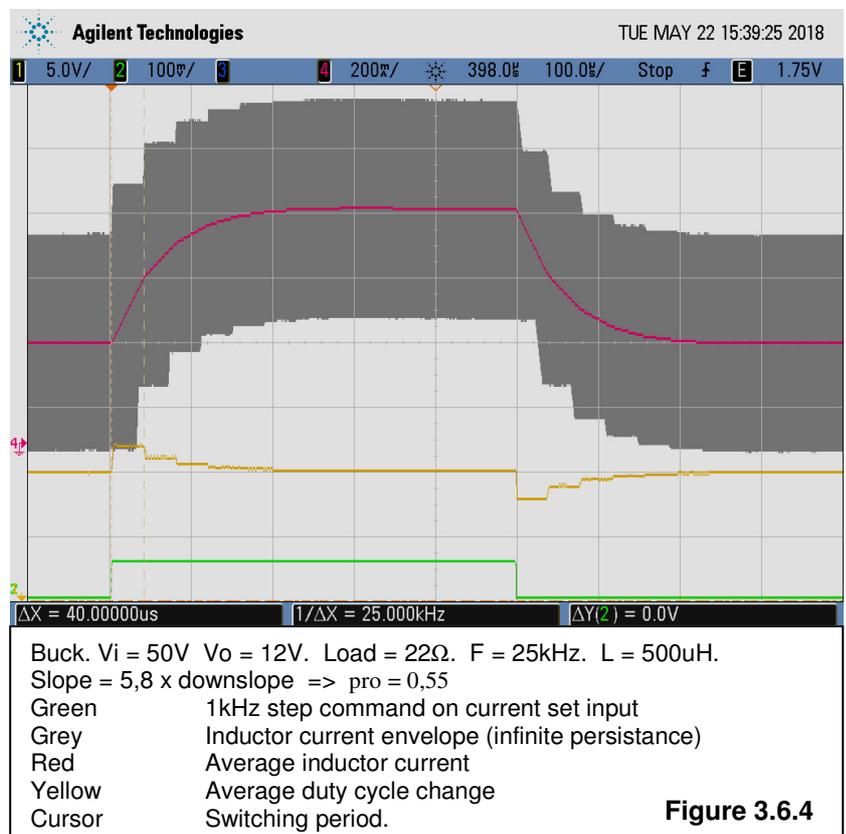
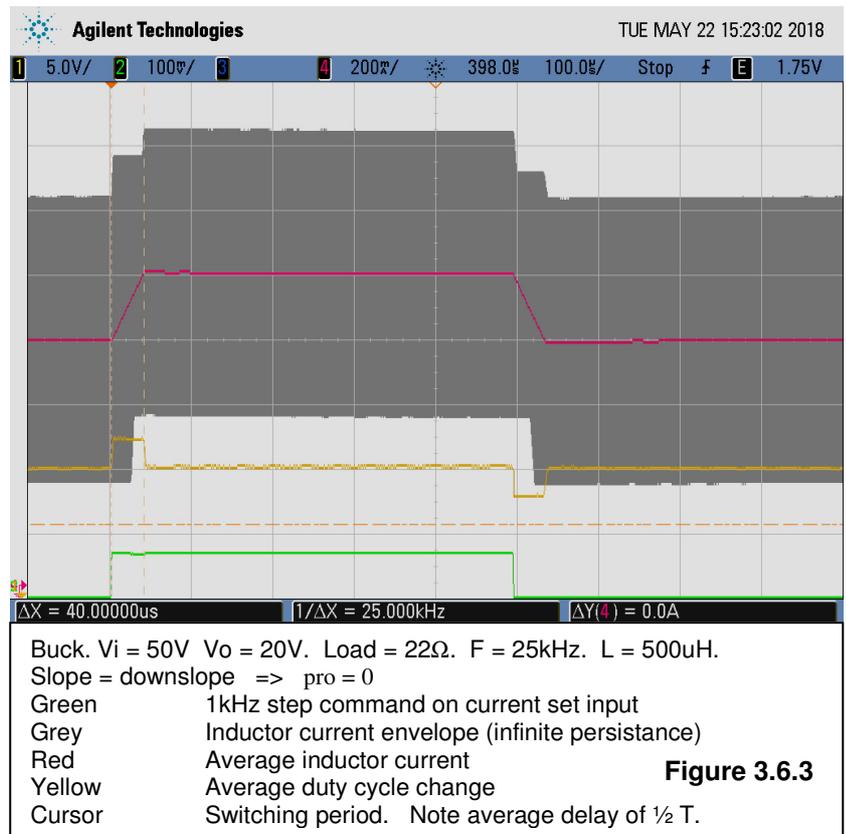
For the first and second experiment the average inductor current does not follow peak current. The difference is the subharmonic ringing. For the third and fourth experiment it could be fair to say that peak and average current follow each other somehow.

It takes a bright mind to figure out these pictures by human brain activity. It would even be difficult to see it in a simulator.

Our first task is now to write the transfer equation for a system having the red average current curves as its step response.

There are surely several ways this can be done. We will try to keep it simple.

We start with the ringing case. And then find that the derived equation works for all cases, ringing or exponential or even oscillating.



OK, figure 3.6.5 shows the function $I_{av}(t)$ that we must transform. Remember that $pro < 0$ for the ringing case. An easy way is to find the derivative $f(t)$, then use the rule that $Laplace(f(t)) = s \cdot Laplace(I_{av}(t))$ or $I_{av}(s) = \frac{1}{s} \cdot f(s)$

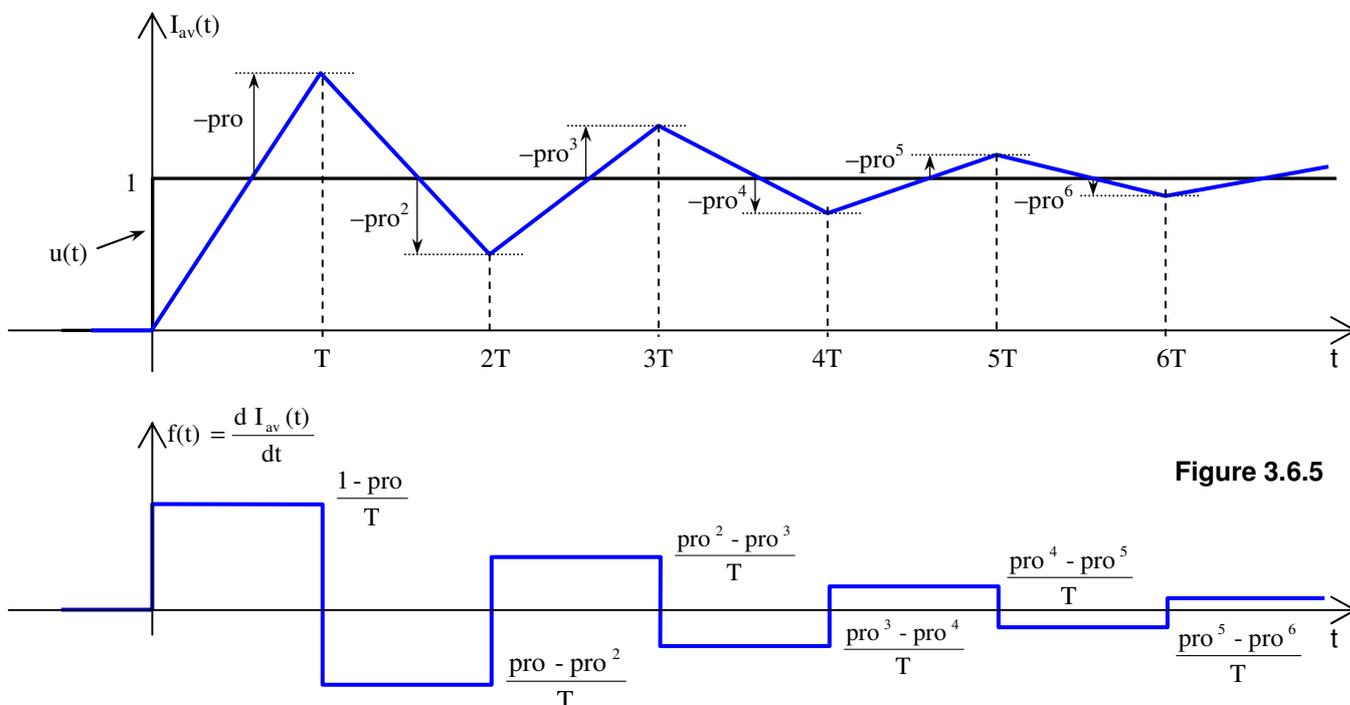


Figure 3.6.5

And then use the other rule that the transfer function $g(s)$ for the system is $s \cdot I_{av}(s)$ as explained with equation (3.5.6). Therefore $g(s) = f(s) = Laplace(f(t))$.



Figure 3.6.6

If we define the pulse function $Pulse(t) = 1$ for $0 \leq t < T$ and 0 otherwise, then $f(t)$ can be seen as an infinite sequence of exponentially decaying pulses, each with a width of T .

$$f(t) = \frac{1-pro}{T} \cdot Pulse(t) + \frac{pro-pro^2}{T} \cdot Pulse(t-T) + \frac{pro^2-pro^3}{T} \cdot Pulse(t-2T) + \frac{pro^3-pro^4}{T} \cdot Pulse(t-3T) + \dots$$

$$f(t) = \frac{1-pro}{T} \cdot \left(Pulse(t) + pro \cdot Pulse(t-T) + pro^2 \cdot Pulse(t-2T) + pro^3 \cdot Pulse(t-3T) + \dots \right) \quad (3.6.1)$$

Using (3.4.5) on each of these pulses and summing:

$$f(s) = \frac{1-pro}{T} \cdot \left(\frac{1-e^{-sT}}{s} + pro \cdot \frac{1-e^{-sT}}{s} \cdot e^{-sT} + pro^2 \cdot \frac{1-e^{-sT}}{s} \cdot e^{-2sT} + pro^3 \cdot \frac{1-e^{-sT}}{s} \cdot e^{-3sT} + \dots \right)$$

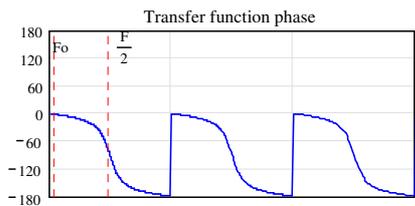
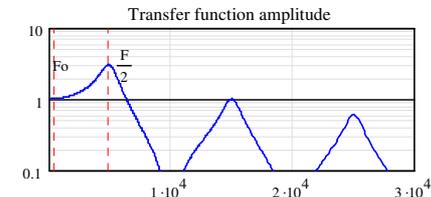
$$f(s) = \frac{1-pro}{T} \cdot \frac{1-e^{-sT}}{s} \cdot \left(1 + pro \cdot e^{-sT} + pro^2 \cdot e^{-2sT} + pro^3 \cdot e^{-3sT} + \dots \right)$$

Using again that $1 + x + x^2 + x^3 + x^4 + \dots = \frac{1}{1-x}$:

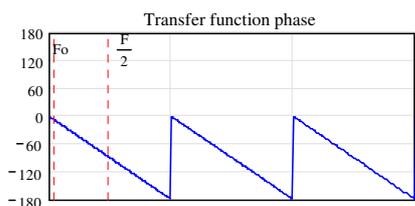
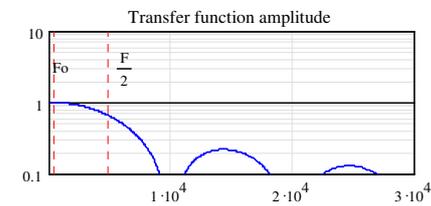
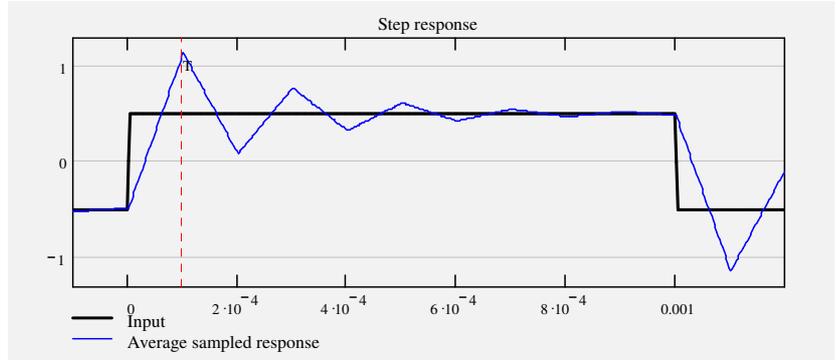
$$g(s) = f(s) = \frac{Rsens \cdot i_L(s)}{v_g(s)} = \frac{1-e^{-sT}}{s \cdot T} \cdot \frac{1-pro}{1-pro \cdot e^{-sT}} \quad (3.6.2)$$

This is our result. $g(s)$ = sample & hold function multiplied by the previously found square ringing transfer function. For $pro = 0$ we get the sample & hold equation (3.4.6) ☺

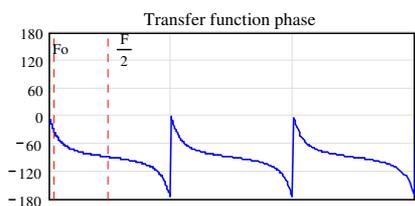
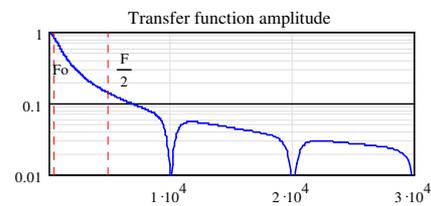
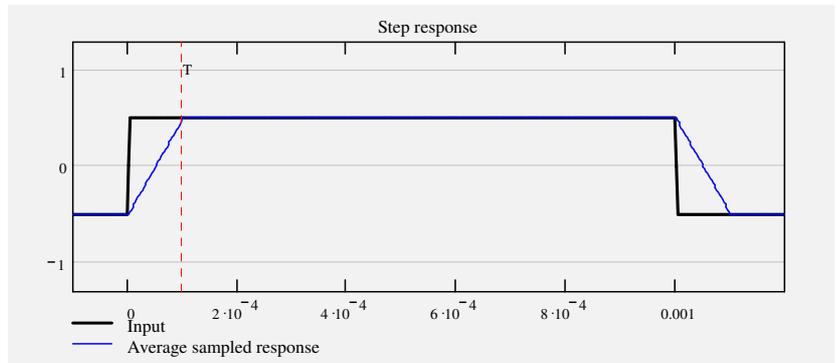
Some plots of this result for $g(s)$ at 10kHz switching frequency:



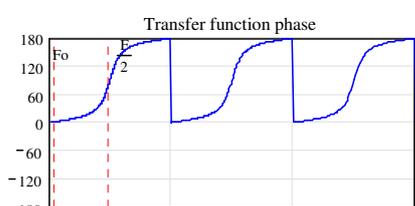
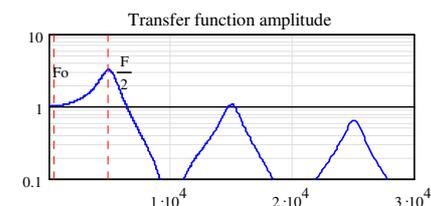
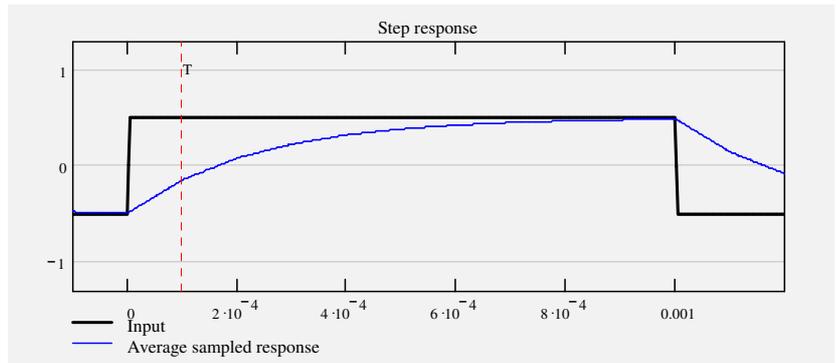
pro = -0.65



pro = 0



pro = 0.65



pro = -1.5

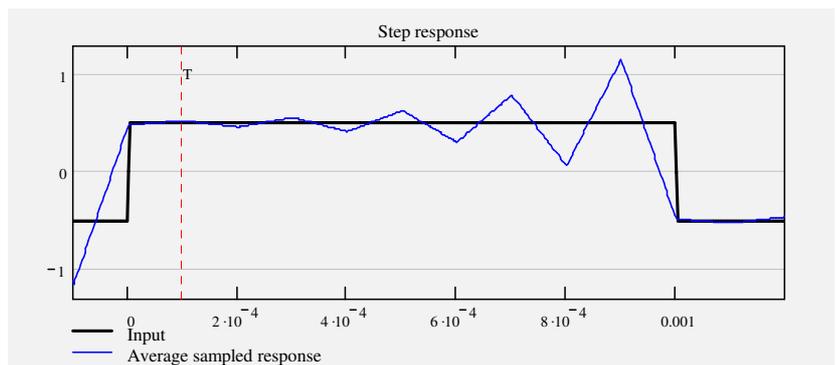


Figure 3.6.7

3.7 How to implement the result in a loop calculator

We are nearly ready to find a way to implement this simple looking result in the existing loop calculators. But there is one more thing to consider. One thing that took me a while to figure out.

$g(s)$ is indeed the high frequency gain of the power stage, which is perfectly proved by these step responses. But with the selected approach $g(s)$ is not directly usable in our model containing the modulator gain expression.

For all pulse width modulated converters in CCM we found the modulator gain expression (2.2.1) to be a governing expression in the loop description:

$$\delta(s) = \frac{v_g(s) - R_{sens} \cdot \hat{i}_L(s)}{V_{pp}} \quad (3.7.1) = (2.2.1)$$

It contains peak inductor current $\hat{i}_L(s)$ which makes this equation valid from pulse to pulse as well as in the long term.

However, what must be used to calculate the output voltage or current is average inductor current pr. cycle, not peak current. And we just found that average current pr. cycle does not completely follow peak current. If we could somehow replace the peak current in (2.2.1) with an expression containing average current pr. cycle at high frequency, we would be done.

The previous discussion presupposes that there is no significant change of output (and input) voltage while the subharmonic ringing is observed. This assumption is reasonable in an SMPS with a low impedance output capacitor. Therefore it is fair to let the subharmonic model only describe the fast changing currents from cycle to cycle, while the already found equations (2.5.5) and (2.5.7) should continue to describe what happens with slower speed.

A way to find the ratio $\frac{\hat{i}_L(s)}{i_L(s)}$ is to combine the modulator gain with basic buck converter equation (2.1.8):

$$\frac{i_L(s)}{\delta(s)} = \frac{V_i}{s \cdot L + R_L + Z_{load}(s)} \quad (3.7.2) = (2.1.8)$$

However, in (3.7.2) Z_{load} and R_L should now be set to zero to agree with the assumption that the output voltage of the basic buck stage does not change. If we don't we get wrong results at low frequency.

Modulator gain:
$$\delta(s) = \frac{v_g(s) - R_{sens} \cdot \hat{i}_L(s)}{V_{pp}} \quad (3.7.1)$$

From (3.7.2):
$$\delta(s) = i_L(s) \cdot \frac{s \cdot L}{V_i} \quad (3.7.3)$$

Equating the two right hand sides:
$$\hat{i}_L(s) = \frac{v_g(s)}{R_{sens}} - i_L(s) \cdot \frac{s \cdot L}{R_{sens}} \cdot \frac{V_{pp}}{V_i} \quad (3.7.4)$$

For the average inductor current we already found $g(s)$ in (3.6.2) so that
$$R_{sens} \cdot i_L(s) = v_g(s) \cdot g(s) \quad (3.7.5)$$

Combining these equations leads to
$$\hat{i}_L(s) = \frac{v_g(s)}{R_{sens}} \cdot \left(1 - g(s) \cdot \frac{s \cdot L}{R_{sens}} \cdot \frac{V_{pp}}{V_i} \right) \quad (3.7.6)$$

and combining (3.7.5) and (3.7.6) leads to the correction term:
$$HF_{cor}(s) = \frac{\hat{i}_L(s)}{i_L(s)} = \frac{1}{g(s)} - \frac{s \cdot L}{R_{sens}} \cdot \frac{V_{pp}}{V_i} \quad (3.7.7)$$

Aha the correction we need involves not just $g(s)$ but something more.

Let's check the peak current by plotting the bracket in (3.7.6) and especially its step response.

Plots of $\left(1 - g(s) \cdot \frac{s \cdot L}{R_{sens}} \cdot \frac{V_{pp}}{V_i}\right)$ (red) together with the average inductor current function (blue):

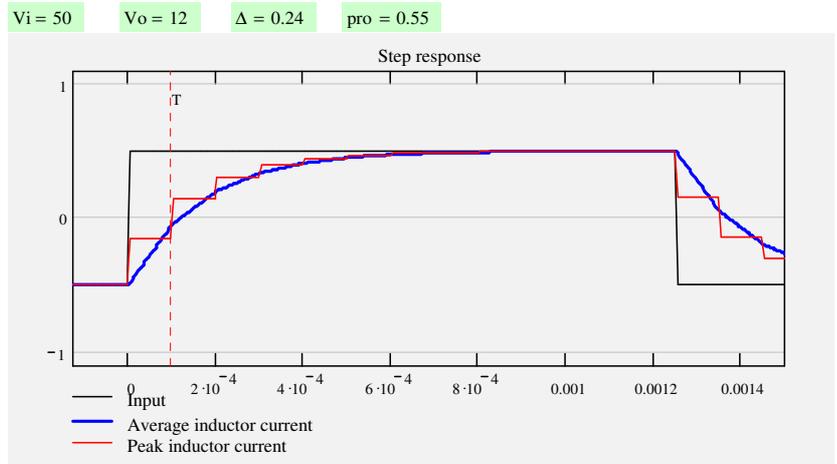
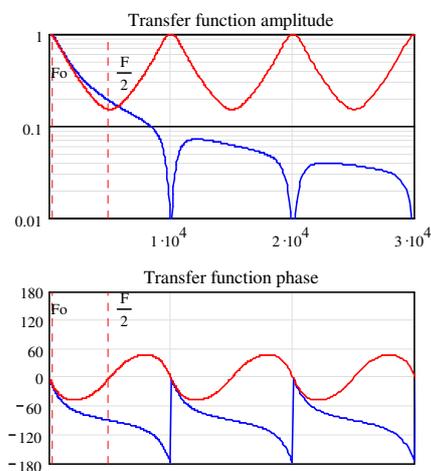
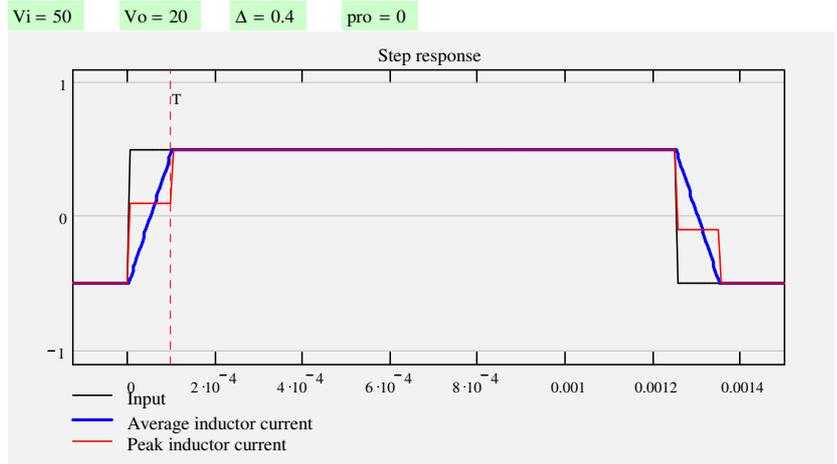
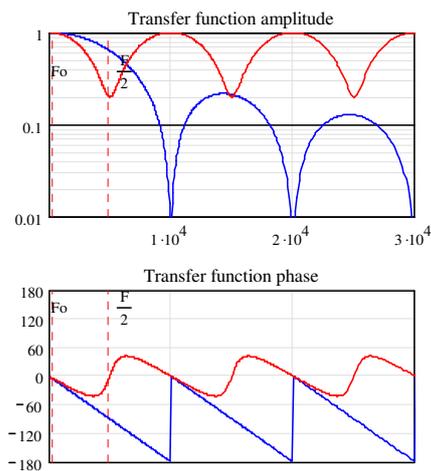
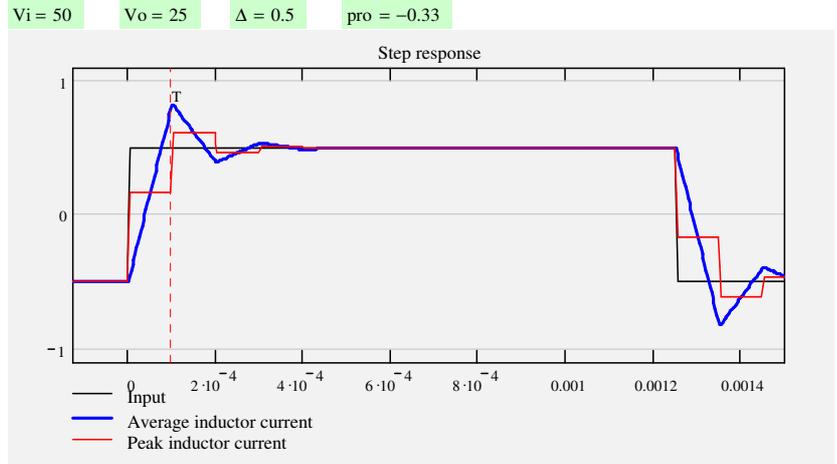
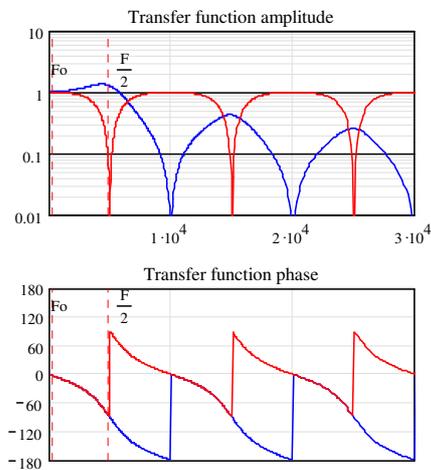


Figure 3.7.1

For these plots I selected data aligned with those in the scope plots, except switching frequency and step frequency. Compare the calculated peak current with the upper envelope in the scope plots.

Isn't it amazing what math can do?

A short discussion of the observations in these plots and especially the scope plots will be appropriate. Here are two forms of the modulator gain:

$$\delta(s) = \frac{v_g(s) - R_{sens} \cdot \hat{i}_L(s)}{V_{pp}} \qquad R_{sens} \cdot \hat{i}_L(s) = v_g(s) - \delta(s) \cdot V_{pp} \qquad (3.7.8)$$

The last one states that peak current follows the control signal minus $V_{pp} \cdot$ duty cycle deviations. This is exactly what we see in the scope plots. And if $V_{pp} = 0$, there is nothing to subtract, so peak current follows control signal.

It is remarkable that we have not done any new assumptions or approximations. (3.7.7) covers all situations, ringing, critically damped or highly overdamped. Even pure duty cycle control, however we then unfortunately will divide by $R_{sens} = 0$.

We could solve this small problem and go ahead with (3.7.7). It would be perfect.

But simplifications can still be made, and there are more interesting things to be learned. Hang on just a little while more.

During check plots it appeared that $HF_{cor}(s)$ does not depend on neither L , R_{sens} , nor V_{pp} , only on the ratio $\Delta = V_o/V_i$ and the switching frequency. That is not at all evident from (3.7.7), since these variables are part of the equation, and $g(s)$ also depends on them.

Is that a coincidence? No it isn't. At this moment it appeared to me that the relation between peak and average current pr. cycle at any frequency must be an inherent property of the power cell, a property which does not rely on control methods. It is the same, whether it is peak current controlled or duty cycle controlled or anything in between.

OK, if this is true, we could try to find $HF_{cor}(s)$ in an alternative way: calculate it in a special situation where it is easy. This special situation is with $V_{pp} = 0$, that is pure current mode control, in which peak current is exactly = control signal divided by R_{sens} . In this situation we know that

$$R_{sens} \cdot \hat{i}_L(s) = v_g(s)$$

$$R_{sens} \cdot i_L(s) = g(s) \cdot v_g(s)$$

so therefore
 agreeing with (3.7.7).

$$HF_{cor}(s) = \frac{\hat{i}_L(s)}{i_L(s)} = \frac{1}{g(s)} \Bigg|_{V_{pp} = 0} \qquad (3.7.9)$$

For $V_{pp} = 0$ - from (3.2.1):

$$pro_o = \frac{-\text{downslope}}{\text{upslope}} = \frac{-V_o}{\left(\frac{V_i - V_o}{L}\right)} = \frac{-V_o}{V_i - V_o}$$

and using $g(s)$ from (3.6.2):

$$HF_{cor}(s) = \frac{s \cdot T}{1 - e^{-s \cdot T}} \cdot \frac{1 + \frac{V_o}{V_i - V_o} \cdot e^{-s \cdot T}}{1 + \frac{V_o}{V_i - V_o}} = s \cdot T \cdot \left(\frac{1}{1 - e^{-s \cdot T}} - \frac{V_o}{V_i} \right) \qquad (3.7.10)$$

What a simple expression, albeit still not easily seen through. The first term is the reciprocal of a sample & hold function. But what does that imply? Don't speculate too much. A math calculator won't care, it just calculates it.

In a buck converter we can also write (3.7.11)

$$HF_{cor}(s) = s \cdot T \cdot \left(\frac{1}{1 - e^{-s \cdot T}} - \Delta \right)$$

Replacing V_o/V_i with Δ is smart because the progression factor pro is always the same for the same Δ , regardless if we are working with buck, boost or buck-boost. This makes (3.7.11) directly usable in all three converter types.

And after this simplification we no longer divide by zero at any time.

Having seen this, (3.7.7) can of course be reduced to (3.7.10), but it is tedious work: first insert V_i and V_o in the slopes, insert slopes in pro , then insert pro in $g(s)$ and use normal algebra to reduce it. At first it looks as if it

never stops growing in size, hard to see that it can end as simple as (3.7.10). Embarrassingly, I needed some help to come through it myself.

The rest is simple.

Since $\hat{i}_L(s) = HF_{cor}(s) \cdot i_L(s)$ from (3.7.7) and since $\hat{i}_L(s)$ always appears multiplied to R_{sens} , we can define a new complex and strange sense resistor

$$R_{sens}(s) = R_{sens} \cdot HF_{cor}(s) \quad (3.7.12)$$

and just replace R_{sens} with $R_{sens}(s)$ in the equations (2.5.5) and (2.5.7).

That's all folks 😊

We can forget about all the $h(s)$, $f(s)$, $g(s)$ etc. stuff again. (3.7.11) is the only thing we need. $h(s)$, $f(s)$, $g(s)$ etc. were useful during the progress towards (3.7.10), and I have certainly learned new things and revived others from the engineering school while doing all that exercise.

3.8 The analog way of thinking

For those who would also like to see what an analog model would look like, I will briefly go through some derivations to come to an analog model with more familiar formulae for analog engineers. But it will not be simpler, on the contrary.

An analog model for the subharmonic ringing is that of a 2nd order low pass filter with a DC gain of 1. This filter has the well known transfer function

$$g(s) = \frac{\omega_o^2}{s^2 + \frac{\omega_o}{Q} \cdot s + \omega_o^2} \quad (3.8.1)$$

where ω_o is the radial "resonance" frequency and Q is the quality factor. Ringing (multiple zero crossings) occurs if $Q > \frac{1}{2}$. ω_o is assumed to be at half the switching frequency, so Q is the only quantity we need to find, based on the ringing progression factor pro defined in (3.2.2).

If the poles of the 2nd order denominator are pole₁ and pole₂ respectively, then the inverse Laplace transform will be, according to a math handbook:

$$g(t) = \begin{cases} \omega_o^2 \cdot \frac{e^{\text{pole}_1 \cdot t} - e^{\text{pole}_2 \cdot t}}{\text{pole}_1 - \text{pole}_2} & \text{if } \text{pole}_1 \neq \text{pole}_2 \\ \omega_o^2 \cdot t \cdot e^{\text{pole}_1 \cdot t} & \text{if } \text{pole}_1 = \text{pole}_2 \end{cases} \quad (3.8.2)$$

The upper part is valid for $Q \neq \frac{1}{2}$ i.e. for both ringing and non-ringing responses. The lower part is valid for $Q = \frac{1}{2}$ at the limit case between ringing and non-ringing responses.

$g(t)$ will be equal to the response of a unit dirac impulse.

We need to evaluate $g(t)$ to find the relation between pro and Q.

A lot of complexity is hidden in (3.8.2). No-one can see from this expression what it really does. So let us take it apart to see what's inside.

We know from school that the 2nd order equation $x^2 + B \cdot x + C = 0$

has the following poles: $\text{pole}_1 = \frac{-B + \sqrt{D}}{2}$ $\text{pole}_2 = \frac{-B - \sqrt{D}}{2}$ (3.8.3)

where $B = \frac{\omega_o}{Q}$, $C = \omega_o^2$ and the discriminant $D = B^2 - 4C = \omega_o^2 \cdot \left(\frac{1}{Q^2} - 4\right)$ (3.8.4)

In the ringing case $Q > \frac{1}{2}$ so D is negative. Inserting (3.8.3) and using Euler's equation $\sin(x) = \frac{e^{j \cdot x} - e^{-j \cdot x}}{2j}$

$$g(t) = \omega_o^2 \cdot \frac{e^{\frac{-B+j\sqrt{|D|}}{2} \cdot t} - e^{\frac{-B-j\sqrt{|D|}}{2} \cdot t}}{j\sqrt{|D|}} = \omega_o^2 \cdot e^{\frac{-B}{2} \cdot t} \cdot \frac{\left(e^{\frac{j\sqrt{|D|}}{2} \cdot t} - e^{\frac{-j\sqrt{|D|}}{2} \cdot t} \right)}{j\sqrt{|D|}} = \omega_o^2 \cdot e^{\frac{-B}{2} \cdot t} \cdot \frac{2}{\sqrt{|D|}} \cdot \sin\left(\frac{\sqrt{|D|}}{2} \cdot t\right)$$

Inserting B, C, and D from (3.8.4):
$$g(t) = \omega_o^2 \cdot \frac{e^{\frac{-\omega_o}{2Q} \cdot t}}{\sqrt{1 - \frac{1}{4Q^2}}} \cdot \sin\left(\omega_o \cdot \sqrt{1 - \frac{1}{4Q^2}} \cdot t\right) \quad (3.8.5)$$

In the non-ringing case $Q < \frac{1}{2}$ and $g(t)$ will contain a "sinh" expression instead of "sin". The hyperbolic sinh is a non-ringing function. We do not need this part of the math.

From (3.8.5) we see that the response to a dirac impulse is an exponentially decaying sine wave with the angular frequency and decay factor

$$\omega_{\text{ring}} = \omega_o \cdot \sqrt{1 - \frac{1}{4Q^2}} \quad \text{decay}(t) = e^{\frac{-\omega_o}{2Q} \cdot t} \quad (3.8.6)$$

The ringing frequency ω_{ring} differs from the resonance frequency ω_b . They are identical for high Q, but the ringing frequency of an analog resonating system will decrease towards zero, as Q approaches $\frac{1}{2}$. This will probably surprise many engineers. However, when it occurs, the resonance is so damped that it is difficult to see the zero crossings anyway.

We know that subharmonic ringing always occurs at precisely $F/2$, also when the ringing is heavily damped. So there is an error in the analog model regarding ringing frequency. We can fix it by using a corrected resonance frequency:

$$\omega_o = \frac{2\pi \cdot \frac{F}{2}}{\sqrt{1 - \frac{1}{4Q^2}}} \quad (3.8.7)$$

The decay equation can be used to find the relation between pro and Q. (3.8.7) must be used in order to make Q go to $\frac{1}{2}$ when pro moves from -1 to 0. Inserting (3.8.7) in (3.8.6) gives

$$\text{decay}(t) = e^{\frac{-\pi \cdot F}{\sqrt{4 \cdot Q^2 - 1}} \cdot t} \quad (3.8.8)$$

Now we can find pro by setting $\text{pro} = -\text{decay}(T)$:

$$\text{pro} = -e^{\frac{-\pi}{\sqrt{4 \cdot Q^2 - 1}}} \quad (3.8.9)$$

and solve with respect to Q:
$$Q = \sqrt{\left(\frac{\pi}{2 \cdot \ln(-\text{pro})}\right)^2 + \frac{1}{4}} \quad (3.8.10)$$

(3.8.10) is plotted in figure 3.8.1.

Unfortunately we haven't covered the case with subharmonic self oscillation. When the power cell oscillates, its pro becomes < -1 and Q becomes negative.

In (3.8.9) negative Q gives same result as positive Q.

Therefore, for $\text{pro} < -1$ we are better off using the uncorrected equation instead of (3.8.8):

$$\text{decay}(t) = e^{\frac{-\pi \cdot F}{2Q} \cdot t} \quad (3.8.11)$$

setting $\text{pro} = -\text{decay}(T)$:

$$\text{pro} = e^{\frac{-\pi}{2Q}} \quad (3.8.12)$$

Q for subharmonic self oscillation:

$$Q = \frac{-\pi}{2 \cdot \ln(-\text{pro})} \quad (3.8.13)$$

One small thing still remains to be done.

The analog model results in a damped or growing sine wave. The sampled model gives a damped or growing triangle waveform. We should adjust the analog model to have the same fundamental amplitude of the ringing frequency component.

The fundamental of a sine with amplitude 1 is 1.

The fundamental of a triangle with amplitude 1 is $\frac{8}{\pi^2}$.

But if we just multiply (3.8.1) with this factor, it will no longer have a DC gain of 1. Instead if we multiply $\frac{8}{\pi^2}$ on the Q-factor it looks better.

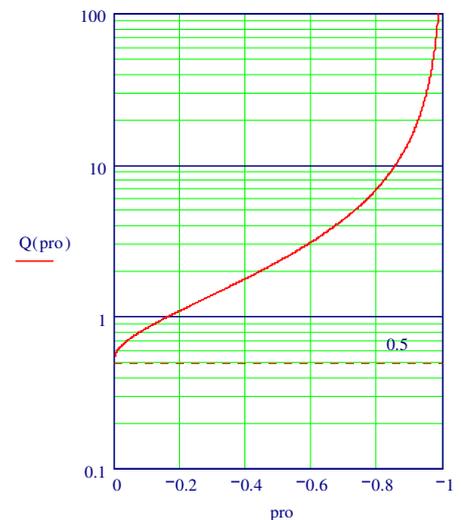
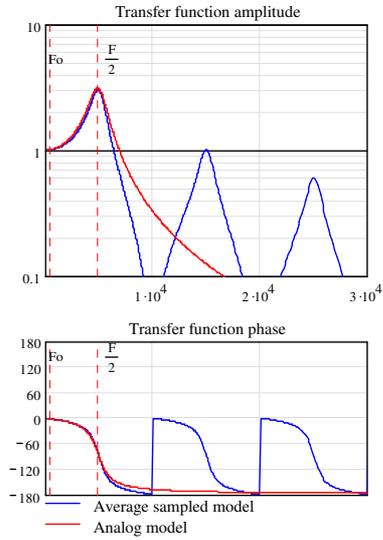
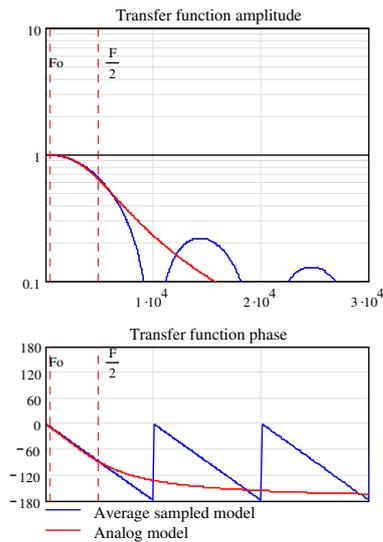
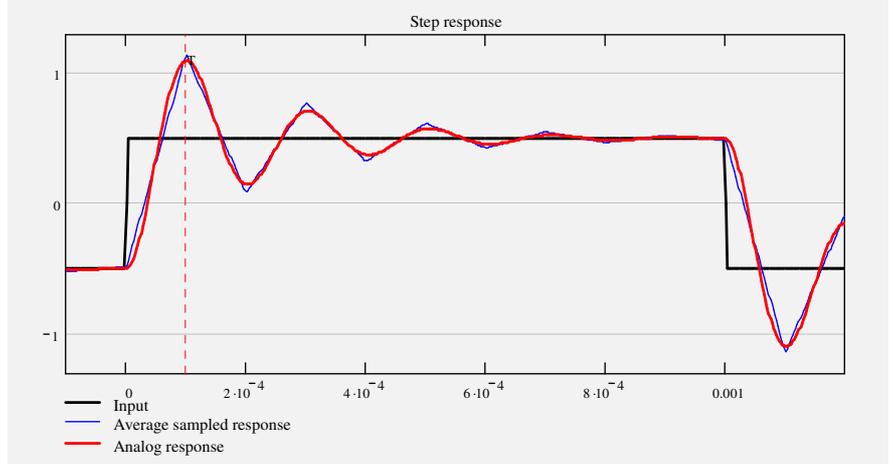


Figure 3.8.1

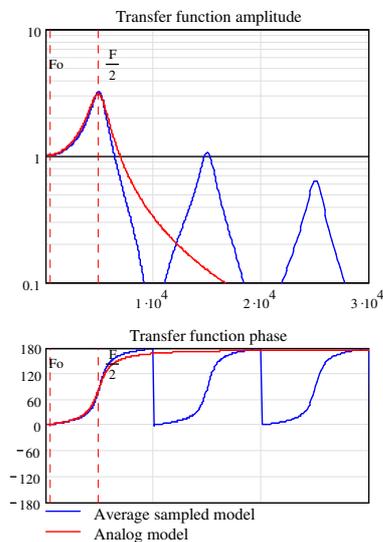
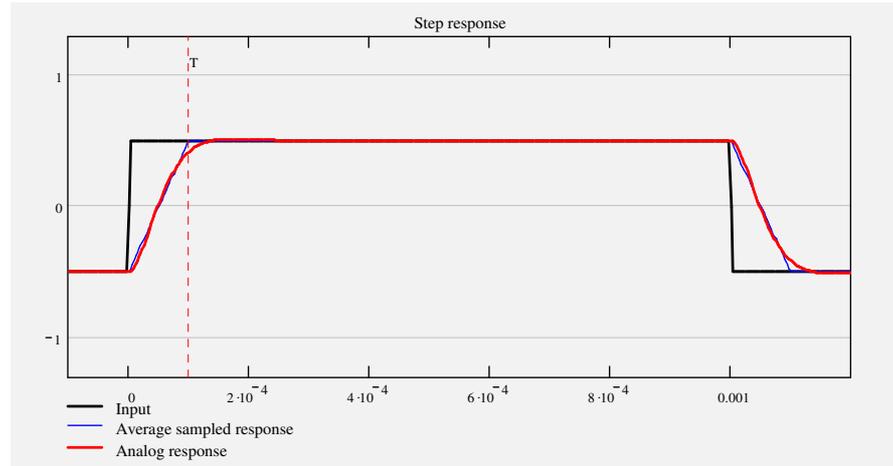
Some plots of the analog results compared to sampled ones.



pro = -0.65



pro = 0



pro = -1.5

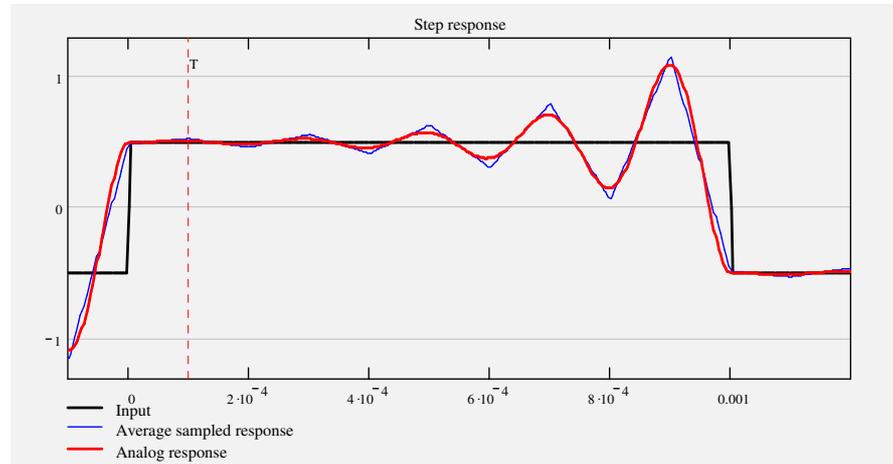


Figure 3.8.2

Inspired from the previous section, what we must do is to find the correction factor HFcor for the analog model and multiply it to Rsens.

HFcor was found to be independent on control method and it was found to be equal to $1/g(s)$ for $V_{pp} = 0$. This means we do not have to bother with equations for $Q < 1/2$ because with $V_{pp} = 0$ Q is always $> 1/2$. Therefore we will not derive equations to calculate an analog plot for $Q < 1/2$ ($pro > 0$) for the previous page, as we did in figure 3.7.1 lower graph.

All those plots were just for understanding and check, and are not needed in the loop worksheets.

So - to build the analog model:

Start with finding the pro factor for $V_{pp} = 0$: $pro_o = \frac{-\text{downslope}}{\text{upslope}}$ (3.8.14)

pro_o is generally different from pro .

Then define the Q-factor for $V_{pp} = 0$: $Q_o = \frac{8}{\pi^2} \cdot \begin{cases} \sqrt{\left(\frac{\pi}{2 \cdot \ln(-pro_o)}\right)^2 + \frac{1}{4}} & \text{if } pro_o > -1 \\ \frac{-\pi}{2 \cdot \ln(-pro_o)} & \text{if } pro_o < -1 \\ 10^{10} & \text{if } pro_o = -1 \end{cases}$ (3.8.15)

Gain from control to average inductor current at $V_{pp} = 0$: $g_o(s) = \frac{1}{1 + \frac{s}{\omega_o \cdot Q_o} + \frac{s^2}{\omega_o^2}}$ (3.8.16)

HF correction factor for Rsens: $HFcor(s) = \frac{1}{g_o(s)} = 1 + \frac{s}{\omega_o \cdot Q_o} + \frac{s^2}{\omega_o^2}$ (3.8.17)

and finally: $R_{sens}(s) = Rsens \cdot HFcor(s)$ (3.8.18)

Compare equations (3.8.14 - 17) with the simplicity of (3.7.10).

Could the above equations also be simplified like we did with (3.7.10)? I don't think so. And I don't really care because I will use the sampled model.

I hate to admit it, but in this case "digital" wins over "analog".

3.9 Comparing models – a calculated example

Here are three plots of the same buck converter from our three models.

This example demonstrates the value of including the peaking effect at $F/2$. The rightmost picture would lead us to think that this is a fine design, but the subharmonic inclusion tells us that in this case we should add some slope compensation to damp the $F/2$ peak.

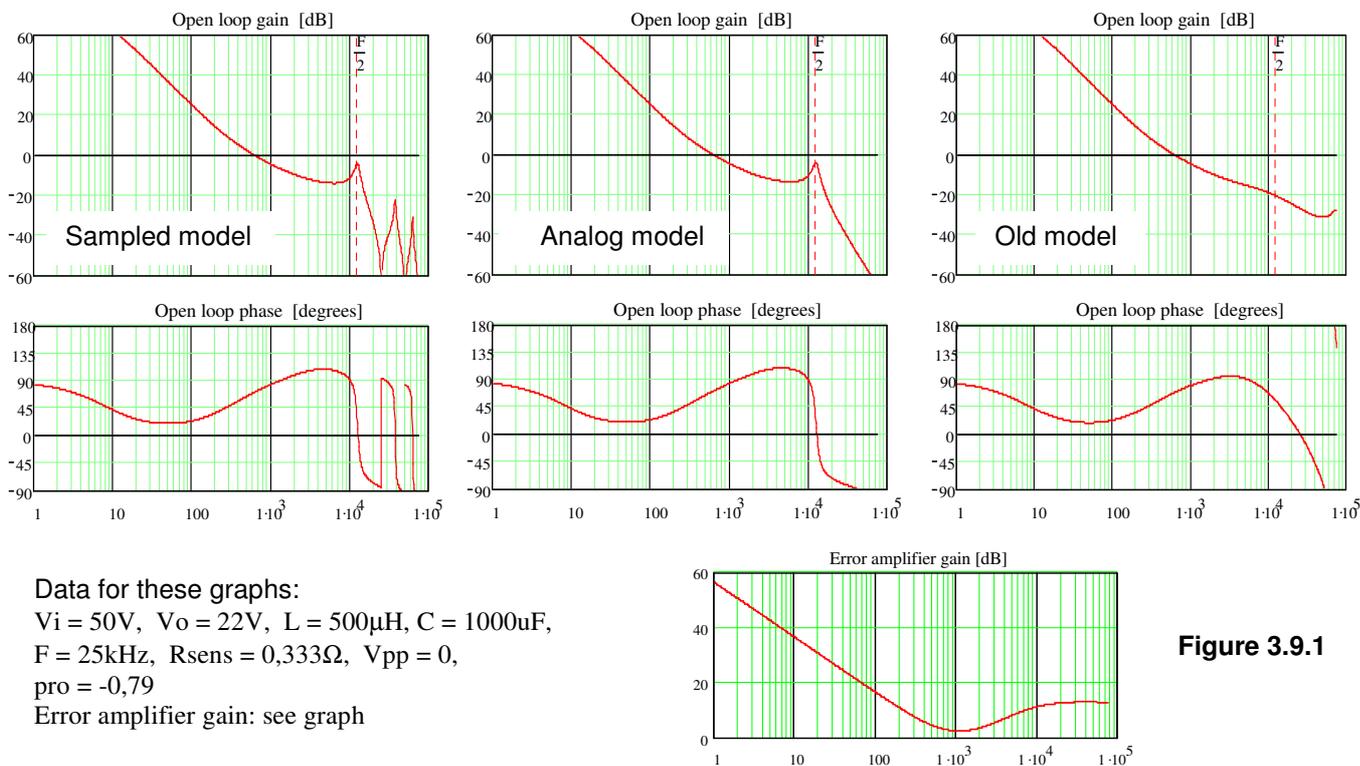


Figure 3.9.1

The plots end at $3 \cdot F$ to see the difference between the sampled model and the analog model. But plotting beyond F does not make any sense. In fact gain and phase data above $F/2$ have no value except to make the $F/2$ peak clearly visible.

Most mathematical models in engineering are more or less an approximation to reality. However, I believe that the models found in the previous pages, especially the sampled model, is a more correct description of reality than anyone could have expected to find. It has been verified with a lot of Simplis simulations of buck and flyback, and up to $F/2$ both simulation and the sampled model agree so well that no difference could be seen in frequency plots. Simplis is a great tool. And it simulates fast. There is a limited version which is free (ref. 13).

3.10 Sweep of control method

The next plots demonstrate what happens for a buck power stage, if we sweep the control from pure CMC to VMC. Output voltage is close to $V_i/2$, therefore the $F/2$ peaking is severe in CMC.

Figure 3.10.1 is a plot of (2.5.5) with R_{sens} corrected with (3.7.11). Figure 3.10.2 is (2.5.7) + (3.7.11).

As we add more slope compensation, the $F/2$ peak collapses.

In the second half we leave the slope unchanged but decrease the current sense gain, until we are in pure VMC. In VMC we see the resonance peak of L and C_o .

The first plot is gain from control input to inductor current.

Note how little current signal injection is necessary to damp the LC resonance.

The current sense resistor in CMC is 1Ω in this example. Therefore the gain at medium frequencies is $1 A/V$ for CMC.

The drop in gain at low frequencies for $V_{pp} = 0$ (black curve) is related to the ripple correction term explained in chapter 2.5.

Units in the legend are V and Ω .

Further data for this buck power stage is shown under the second plot.

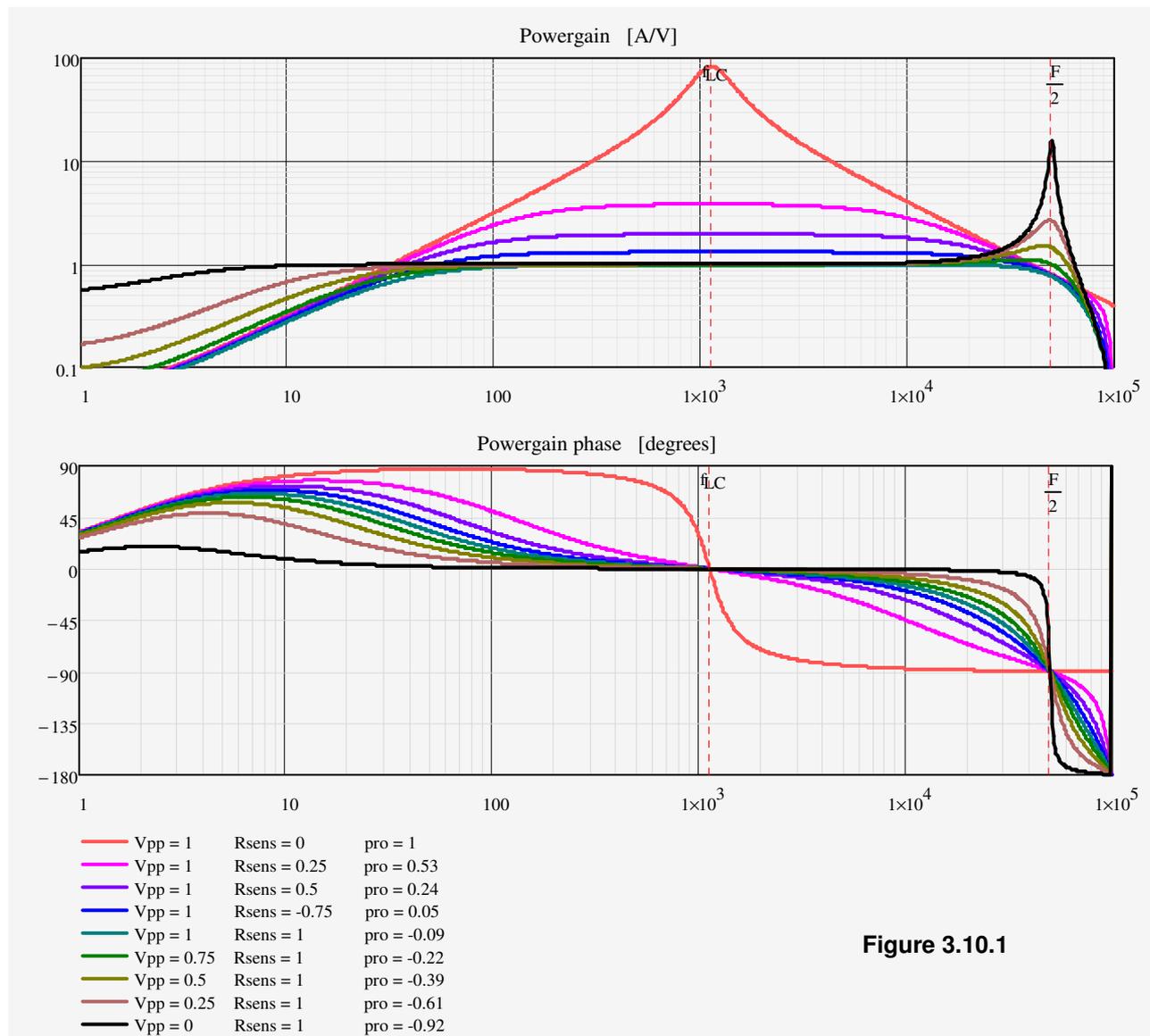


Figure 3.10.1

The second plot is gain from control input to output voltage.

The second plot looks a lot like that of Dr. Ridley which has become known as the logo of his company and as a typical plot from his software (ref. 6). However, my method does not require you to check "Voltage Mode Control" or "Current Mode Control", since the mode of operation is already given by R_{sens} and V_{pp} . Having to specify both leads to the risk of inconsistent inputs.

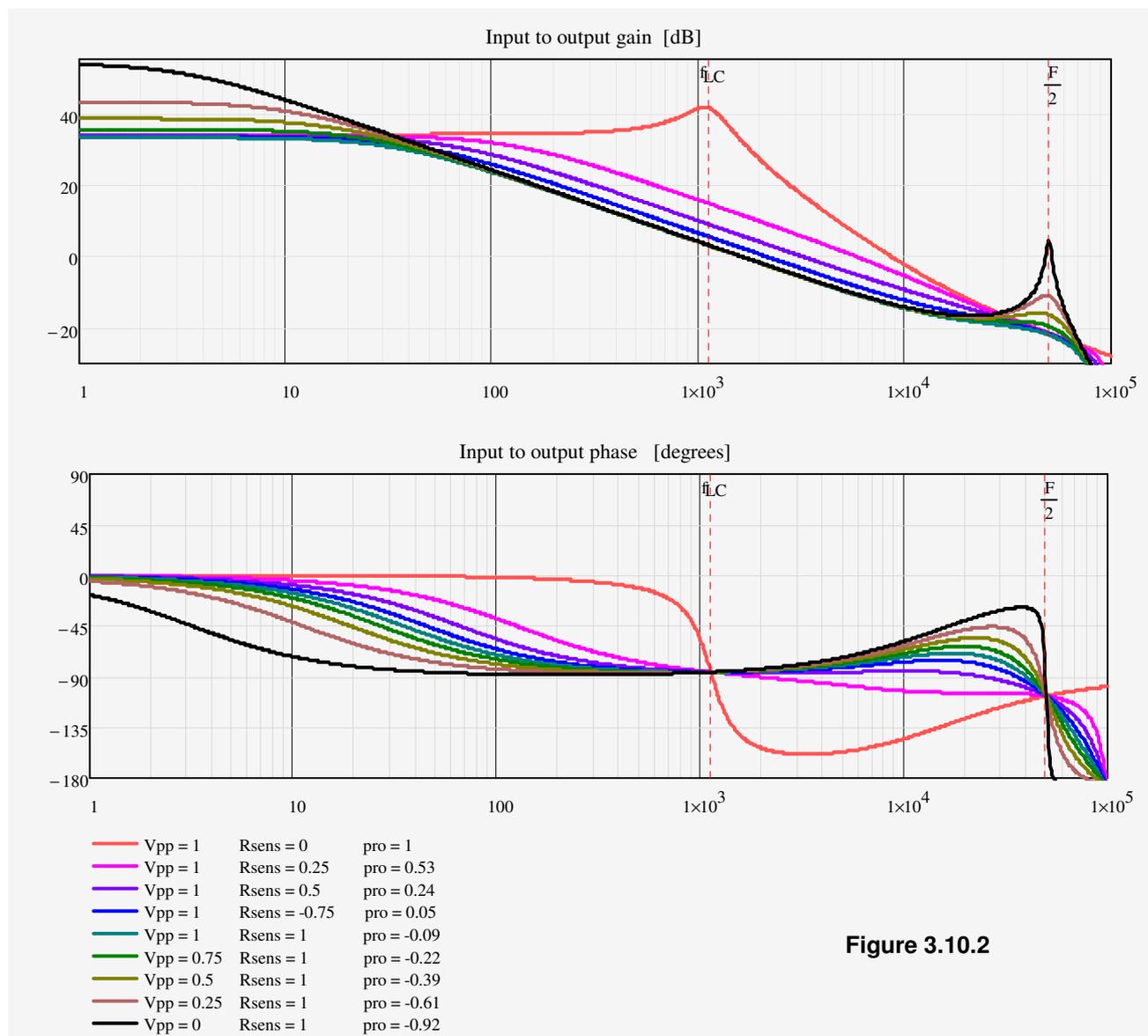


Figure 3.10.2

- Inductor [H], [ohm]: $L \equiv 200 \cdot 10^{-6}$ $R_L \equiv 0.5$
- Output capacitor [F]: $C_o \equiv 100 \cdot 10^{-6}$ $ESR \equiv 0.1$
- Dynamic load resistance [ohm]: $R_{load} \equiv 1000$
- Input and output voltage [V]: $V_i \equiv 50$ $V_o \equiv 24$
- Switching frequency [Hz]: $F \equiv 100 \cdot 10^3$

3.11 Things not covered by this article

In this article I have concentrated on one topic: to study the complex gain function of the buck converter's power stage in CCM with special attention on the subharmonic behaviour. This is one way to start understanding the methods that can be used to make calculators for SMPS feedback loops.

A lot of things are not covered here, for instance:

1. **Boost and buck-boost** power stage gain with the associated **Right Half Plane Zero** as a sub-topic.
2. Derived topologies like **forward** and **flyback** etc.
3. Non-PWM based topologies like **resonance converters**.
4. The power stage gain in **Discontinuous Current Mode**. It can be much different from the gain in CCM. The subharmonic behaviour is absent in DCM.
5. Calculating the closed loop output impedance **Zo** - a subject neglected in most literature.
6. How to add an **LC output filter** and implement it in the calculator. And to predict the open- and closed loop behaviour when the feedback signal is derived from before or after the filter. Or from somewhere else. An LC output filter is often used, and it can have a severe influence on your feedback loop, as well as how you connect the feedback path(s) to it. See more in ref. 11.
7. How to **control output current** instead of voltage. Or how to combine the control of output voltage and current to make a power supply with a pre-determined output resistance.
8. Using the **SMPS as a power amplifier**, i.e. with a fast moving reference as the input signal. How to calculate the (closed loop) gain function versus frequency of such an amplifier.
9. The linear parts of the feedback network: error amplifier, transconductance amplifier, opto coupler, etc.
10. How to calculate the **step load response** of an SMPS or the step control response of an SMPS amplifier, based on the closed loop gain calculations.

Some of these features are described qualitatively in ref. 11.

All of these features are included in my assortment of loop calculator tools, some features however not yet for all topologies. They are built as "open source" in Mathcad, so the user can for instance remove the inverting error amplifier and insert a non-inverting amplifier at any time. Or modify the equations of the linear part to cover the circuits in a dedicated IC. This freedom of use is not offered by any other loop software that I know. Except simulation tools of course, but simulation is quite another thing.

On the other hand it requires some engineering skills to modify or extend the calculators.

3.12 References.

- 1 Unitrode application note U97: Modelling, Analysis and Compensation of the Current-Mode Converter.
<http://focus.ti.com/lit/an/slva101/slva101.pdf>
- 2 Venable Industries: Current Mode Control
<https://venable.biz/uploads/files/05-Technical-Paper-Current-Mode-Control.pdf>
- 3 Ray Ridley's PHD dissertation: A New Small-Signal Model for Current-Mode Control. 1990, 1999, 2015.
Download it from http://www.ridleyengineering.com/images/current_mode_book/CurrentModeControl.pdf
- 4 Rendon Holloway et al: Model Current-Mode Control With Ease and Accuracy. 2008
<https://iie.fing.edu.uy/publicaciones/2008/HE08/HE08.pdf>
- 5 Lloyd Dixon - Texas Instruments: The right half plane zero – a simplified explanation.
- not found on the internet any more
- 6 Ray Ridley: RidleyWorks. SMPS design software replacing the older Power 4-5-6.
Rent it or download an appetizer at
<http://www.ridleyengineering.com/design-center-ridley-engineering.html>
- 7 Dennis Feucht: Current-Loop control in Switching Converters. Part 1 to 7. 2011- 2012.
Part 1: http://www.how2power.com/newsletters/1109/articles/H2PowerToday1109_design_Innovatia.pdf
Part 2-7: find them at <http://www.how2power.com/index.php>.
- 8 Ray Ridley: A More Accurate Current-Mode Control Model.
<https://www.ti.com/seclit/ml/slup122/slup122.pdf>
- 9 Ray Ridley: Current-Mode History and Loose Ends. Part I - V
<http://www.ridleyengineering.com/design-center-ridley-engineering.html>
- 10 Runo Nielsen: Half bridge converter, DC balance with current signal injection. 2012.
http://www.runonielsen.dk/Half_bridge_control.pdf
- 11 Runo Nielsen: Feedback in Switch Mode Power Converters (not covering subharmonic behaviour)
<http://www.runonielsen.dk/Feedback.pdf>
- 12 Vatché Vorpérian: Simplified Analysis of PWM Converters Using Model of PWM Switch,
Part I: Continuous Conduction
Part II: Discontinuous Conduction Mode
IEEE Trans. Aerosp. Electron. Syst., vol. 26, no. 3, pp. 49M96, 1990.
- 13 Simplis simulation software
<https://www.simplistechnologies.com/>

Appendix 1 Perceptions and peculiarities of the PWM modulator

In this paper I have defined a modulator gain expressing the relation between control voltage, duty cycle, and peak current in the presence or absence of a current sensor R_{sens} or a modulator ramp V_{pp} :

$$\text{modulatorgain} = F_m = \frac{\delta(s)}{v_g(s) - R_{sens} \cdot \hat{i}_L(s)} = \frac{1}{V_{pp}} \tag{A1.1}$$

F_m was used in ref. 3 as the name of the modulator gain.

This expression seems to be subject to some controversy among SMPS gurus. The modulator gain has been treated by several authors during the past years, and many seem to disagree with me and with each others regarding its magnitude.

The modulator gain from Ridley (ref. 3) can be re-written as

$$F_m = \frac{\delta(s)}{v_g(s) - R_{sens} \cdot \hat{i}_L(s)} = \frac{1}{V_{pp} + \text{upslope} \cdot T} \tag{A1.2}$$

upslope is the current slope in the on-time multiplied by R_{sens} .

Here the modulator gain is expressed by the sum of slopes of current and compensating ramp, not just the compensation slope as in (A1.1).

Ridley's result seems to make sense at a first glance at figure 2.2.1, since the current upslope and the compensation slope V_{pp} are added in the comparator.

Several earlier and later authors have found other results for the modulator gain (ref. 9 and 4).

Finding the modulator gain at first seems to be a simple task but it is apparently not so simple.

In discussions involving F_m the peak current controlled power cell is often observed as an inner feedback loop where current is measured and used to control the duty cycle, which affects inductor current, so that the sensed peak current coincides with the control signal.

Figure A1.1 is a representation of this inner current loop in a buck converter. The F_m gain box converts voltage to duty cycle. The V_i gain box converts duty cycle back to voltage by multiplying with input voltage.

The open loop gain in this loop can be measured by inserting a small generator in series with the sensed current, and the open loop gain is then v_2/v_1 .

To keep the discussion simple there is no slope compensation in this chapter.

The test generator will show itself only on v_2 (at low frequency, $C_o = \infty$), because the peak value of V_1 must remain at V_g (figure A1.2). Therefore v_1 must be zero so the open loop gain must be infinite, implying that F_m is infinite, which agrees with (A1.1).

This has been the origin of loud discussions, because an infinite open loop gain would always cause the inner current loop to be unstable. We know it isn't, unless $\Delta > 50\%$.

On the other hand, (A1.2) predicts that peak current does not completely follow the control signal, which is clearly not true for $V_{pp} = 0$.

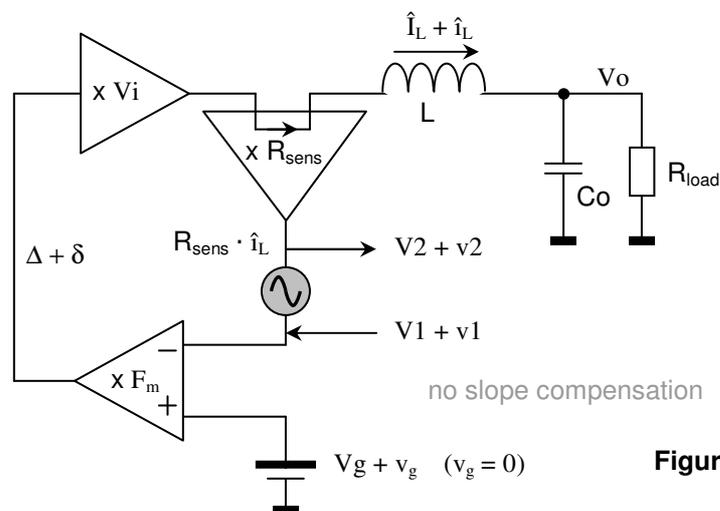


Figure A1.1

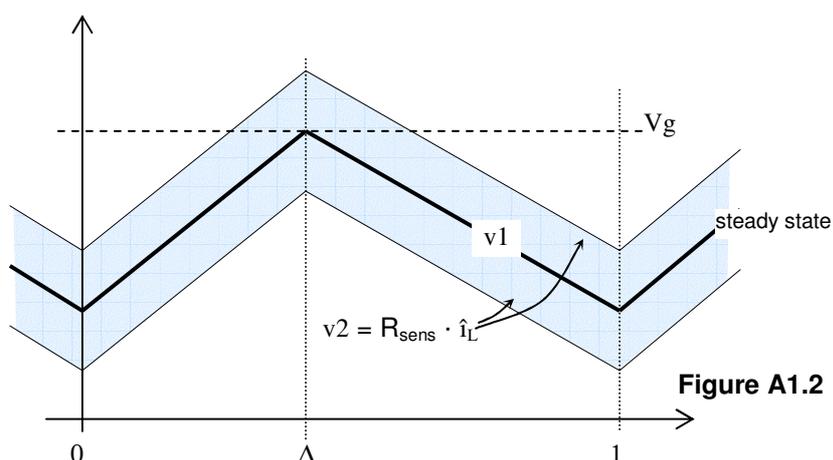


Figure A1.2

It is claimed in ref. 3 and elsewhere that it is incorrect to measure open loop gain in the path with sensed current. Instead it should be measured in a so-called 'digital modulator', where the current loop is opened and a test signal is inserted in a "digital" point (duty cycle is a logic signal) to measure open loop gain. The test generator must then be a pulse extender/contractor.

In this context the open loop gain will be the ratio $\delta 2 / \delta 1$:

$$\text{gain}_{\text{dig}} = \frac{\delta 2}{\delta 1} = \frac{V_i}{Z_{LRC}} \cdot R_{\text{sens}} \cdot F_m$$

Z_{LRC} is the impedance into the inductor from the left hand side.

What is the modulator gain F_m ?

Starting at the steady state, the control duty cycle is perturbed with $\delta 1$. Therefore peak current will be perturbed to \hat{i}_L while average current and output voltage may also increase.

Because the control voltage does not move, this will change the returned duty cycle to $\delta 2$.

Figure A1.4 is an arbitrary snapshot of this.

From the small red line we can write:

$$R_{\text{sens}} \cdot \hat{i}_L = \delta 2 \cdot T \cdot \text{upslope}$$

assuming that slopes have not changed significantly.

So

$$F_m \equiv \frac{\delta 2}{R_{\text{sens}} \cdot \hat{i}_L} = \frac{1}{\text{upslope} \cdot T} = \frac{F}{\text{upslope}}$$

This is identical to Mr. Ridley's F_m with no external ramp (A1.2). It is not infinite.

A more thorough calculation of the loops involving component values etc. can be done, which confirms these results. It runs through the whole buck circuit with R, L, and C included, calculating how $\delta 1$ will affect average and peak current + output voltage, which again affects the returned duty cycle $\delta 2$ - at any modulating frequency. The results fit exactly with Mr. Ridley's published results - as long as we assume that slopes and peak-peak ripple do not change.

Since they do change for finite C_o , the effect from that can be included by adding a dedicated feed forward term from v_o to $\delta 2$, as we did it with the ripple correction term in (2.5.5) and (2.5.7).

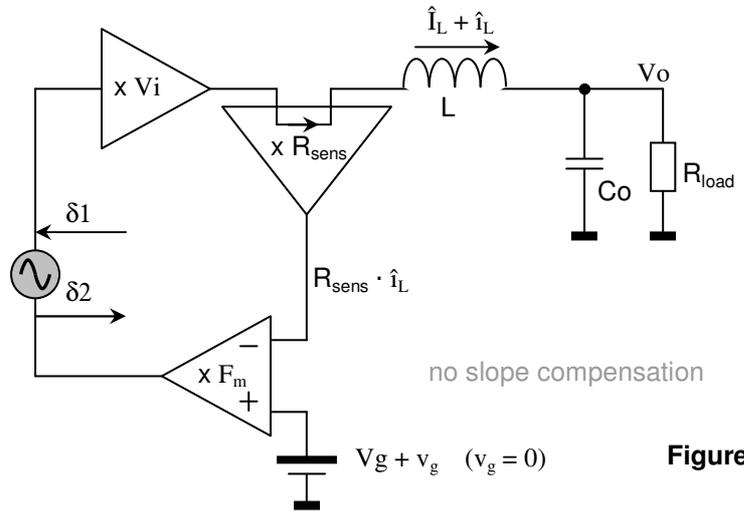


Figure A1.3

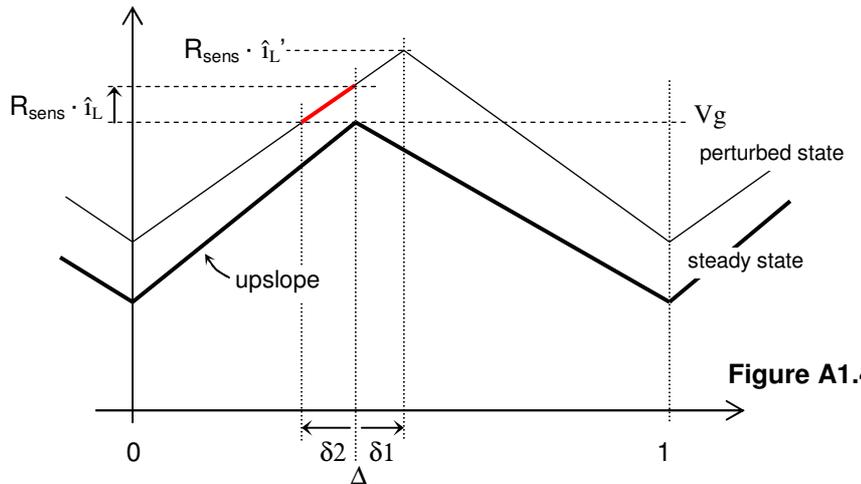


Figure A1.4

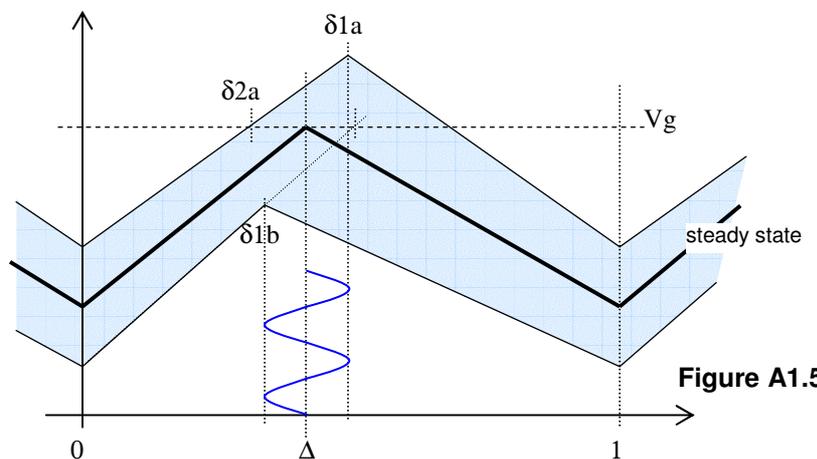


Figure A1.5

Figure A1.5 shows what the whole modulation envelope may look like when δ_1 is modulated with a sine wave at any frequency with constant V_g .

δ_1 swings between δ_{1a} and δ_{1b} , resulting in the returned duty cycle to be δ_{2a} and "non defined" respectively. This modulation makes sense at positive $\delta_1 - \delta_2$ but there will be no returned duty cycle when the modulation goes negative. It would also be problematic to realize the modulator as a pulse contractor: receiving one duty cycle δ_2 and as a result delivering a shorter pulse δ_1 - for this we would need a modulator that can look into the future.

Implementing a realizable digital modulator in a circuit is not straight forward. In a simulator it is a bit easier. Simulation in Simplis has confirmed Dr. Ridley's result for the digital modulator. But with the insertion point as in figure A1.1 both Simplis and real measurements confirm (A1.1) at low frequency, however this model (predicting infinite gain) falls apart at medium and high frequency.

Strangely, we have found two open loop gains for the same system which are not identical. They should be identical because the total open loop gain is the product of the gains of each individual part. Here it seems as if the order of factors in the product makes a difference, which is of course non-sense.

The gain of the PWM modulator seems to be different, seen from those two observation points. The difference is not marginal and it is not just caused by unwanted effects of ripple in the feedback path, as claimed to be the reason to invent the digital modulator.

It seems we are making mistakes when trying to observe the inner current loop as a usual feedback loop. Its action as a feedback loop is really debatable. A feedback system with a single signal path should show the same open loop gain irrespective of where we cut and measure the gain. Or shouldn't it ???

If any of my readers can explain this odd property of the current controlled cell, I will be eager to listen. Life long learning keeps the brain energized.

But I am not really concerned for it. In this presentation I have analyzed the current cell as black box without bothering about its inner properties. What I have found directly - the pro factor - should represent what others would call the closed loop gain of that inner power cell at high frequencies, which is the only interesting property for the design of the outer voltage loop.